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DESIGN OF HIGH-SPEED GNRFET BASED TERNARY LOGIC CIRCUITS

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Abstract

-Utilization of energy sifting to expand the exchanging execution of Graphene Nanoribbon Field-Effect Transistors (GNRFETs) is the main concern of this paper. For similar number of logic bits, multiple valued logic (MVL) be able to communicate a dramatically more prominent number of data than double rationale. Few excellent electromechanical possessions of the Graphene Nano Ribbon Field Effect Transistor (GNRFET), has capacity to control the threshold voltage. GNRFET is be exceptionally encouraging for planning MVL logic gates when contrasted with ordinary and other arising gadget advancements. One of the suggested approaches for accomplishing various voltage levels in the MVL circuit is to change the limit voltage. GNRFET is utilized to show the plan of fundamental ternary logic gates like inverters, TNAND, TNOR and TDECODER. A correlation of GNRFET-established on ternary logic gates and circuits with them in view of exemplary CMOS and GNRFET innovation be situated in utilizing delay, total power and power delay- product (PDP) like measurements. The simulation and analysis are done with the assistance of the H-SPICE tool and a GNRFET 16nm model from the Nanohub site. With proposed design average reduction in transistor count is 1% and 47% in STI and T Decoder respectively. Also achieved average percent reduction in delay 47%, 15%,19% and 5 % for STI, TNAND, TNOR and T Decoder design respectively, this tends to enhancement of the speed of Ternary logic Circuits.

Index Terms---Graphene Nanoribbon Field-Effect Transistor (GNRFET), Ternary Logic Gates, Multi-Valued Logic (MVL), TNOR and TDECODER.

I. INTRODUCTION

A dynamism hole among the transmission also assemblies availabity for chemical bond formation is expected in maximum electromechanical manoeuvres [1]. The electromechanical possessions of semiconductors, like the ON/OFF flow proportion, will be hurt on the off chance that this hole isn't there[1]. Different graphene, a thin strip incised from it, recognised as graphene nanoribbon (GNR), partakes a huge group hole, that be able to lead to nanoscale strategies through a approving ON/OFF current percentage [2], [3]. GNRs really are some of the greatest opportunities aimed at replacing Si in field-effect transistors (FETs) frequencies [1]. Many studies on carrier transport in GNR Field-Effect Transistor (GNRFETs) [5]-[7] have

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been conducted, however the majority of those studies are in the airborne administration [4]–[6]. Huge-path graphene transistors are basically without togetherness, and the origin of the electron pairing underlying the macroscopic quantum phenomenon of electron–phonon (e-ph) smattering appliances have a major impact on their electrical properties [1], [7], [8]. As a result, smooth by the moderately squat frequency, e-ph collaborations essential to have taken into account while simulating a GNRFET [2], [9]. It should be noted that the majority of the research in this area has focused on nanometres which is carbon nanotube (CNT)-based on a semiconductor's device with three connections, capable of application in addition to rectification [2].

As a result of the capacity of MVL reasoning strategies for delivering in a way that becomes quicker and quicker as something that increases becomes greater evidence density than dualistic lucidity, numerous esteemed lucidity which is also called as Multiple Valued Logic (MVL) moreover its solicitations are under widely investigated in the previous decades. Each logic bit in the dualistic especially in computing and electronics system (base 2) will possess dual distinct ethics: low (0) high (1). In the MVL structure (base 3 or more), every cipher be able to possess extra of three or over potential ethics, resulting in much advanced evidence compactness, slighter lucidity posterns, also simplified circuitry. Finally, the fruit of the work is, the MVL system's dynamism depletion, range, then course outflows, as well as further expenditures meant for every jiffy regarding evidence, would be reduced [9]. On behalf of sample, voguish of ternary lucidity structure, each n-bit binary integer is represented by only log32n bits [10], which greatly reduces computing complexity and hence improves the system's power and area efficiency.

Owing of their remarkable electromechanical possessions and combination competences, and practical and influence transistor that would be served as a solo carbon nanotube or an array of carbon nanotubes to work out like network instruments in the place of bulk silicon in the traditional structure which is going to be situated attracting a lot of attention. The carbon-based transistors which are also named after as Carbon Nano Tube Field-Effect Transistor (CNTFET) and Graphene Nano Ribbon Field-Effect Transistor (GNRFET) have become popular research subjects. There are several pieces of literature that work on a carbon nanotube field-effect transistor and the graphene nano-ribbon field effect transistor established on the multivalued reasoning tracks which are better additional for conventional and dual lucidity strategy [9], [10], [12], [13], [10]–[12] and use the verge power regulator process to implement various multivalued lucidity courses those are the better additional for conventional dual lucidity besides reckoning routes. Construction challenges for CNTFETs include opening orientation issues besides unsuitability with architect expertise. Because of the aforementioned logical organisation, GNRFET could have been a better fit as that could be used fashionable surviving organizer Complementary Metal Oxide Semiconductor manufacture development[13]. Resulting, grapheme nano-ribbon field effect transistor gives the impression like a hopeful three valued lucidity besides calculation circuit technology. We provide strategy methodology to the proposal methodology for three valued access along with circuits -founded three valued lucidity courses in this research.

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For the construction of GNR, many fabrication processes have been investigated, including the progression of mechanism from a respective place considered as the repel ink except where it is mandatory for production, organic material. Exciting electromagnetic development of production from respective instruments which is considered as to resist the ink except where it is mandatory for production, and unfastening for tubular huge particles possessing of a hexagonal preparation of mongrelized carbon molecules[14]–[17]. It is able to create graphene nanoribbon with a size of up to 20 nm and irregular edges [20]. In [21], it can be utilized to form a strip besides drawing can be utilized for tapered this one, resulting at a hybrid of lithography and etching. GNR with a width of about 4 nm was created using this technology. Chemical synthesis was employed to make GNRs with a width of less than 2 nm [22]. Additional work of proceeding from the downward to upward organic amalgamation of method which is able to manufacture in the way of involvement of accurate graphene nanoribbon at various properties of asymmetry important in several branches of science and forms with a width for less than 2nm [23] has been developed. [18] and [19] both describe the manufacture of 2 nm wide accurate GNRs. [25] shows how to make such tiny GNRs with flawless edges using the method described there.

This paper makes the following contributions:

• Elucidate various electromechanical possessions of Graphene nano-ribbon practical influenced transistor.

• Using GNRFET, create a variety of fundamental ternary logic gates.

• Compare existing designs on the basis of gradual slowness, energy ingesting, also Power Delay Product (PDP).

Its study can be a follow-up to our recent journal of nanotechnology review [20], that describes a three valued a device that converts direct current electricity for supplying power architecture based on GNRFETs. The basic notion given in [9] is expanded in this study, which gives a broad strategy to implementing grapheme nano-ribbon field effect transistor-established lucidity besides calculation of courses. It is a remainder for the information page which is laid out by way of monitoring. This mathematical description for its three valued lucidity structure is briefly illustrated in Section II. Its functioning value for the grapheme nano-ribbon field effect transistor is explained and in these enterprises for numeral verities regarding three valued paths of lucidly and calculation circuit based on the GNRFET are shown in Section III. Section IV compares the graphene nano-ribbon field effect transistor –established three valued courses to which were established on current skills in terms of both quality and quantity. As a whole, Section V brings important of study to the close with a short-term description of the current effort.

II. GNRFET LOGIC TERNARY SYSTEM

The dualistic digit organisation can be one which has twofold separate reasoning stages: Correct (one) and Wrong (zero). It is traditional possession of the truth-values of truth and falsehood reasoning organization is able to be expanded for the numerous respected reasoning organization with "R" distinct reasoning stages, wherever R > 2. Signal variables such as

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voltage, current, and charge can be used to represent different logic levels. Any of the two prevailing conventions can be used to demonstrate the conventional for distinct logic stages for multi valued logic manoeuvre: unbalanced or balanced. Unbalanced systems are created when a twofold organization be able to increase for particularly throughout expansion can only go in one direction. An unbalanced R-bit multi valued organisation, for example, be able to stand for 0, 1, 2... (R-2) (R-1). This well-adjusted organisation can be defined as an established of numeral figures through the peculiar radix R = 2K+1, such as (-K), (1-K) … 1, 0, 1... (K-1), K [9].

The three valued reasoning organisation can be single procedure of multi-valued logic (MVL) organisation, and there is valuable of R = 3. Resulting familiar resolution for its multi valued MVL organisation, there is instable besides well-adjusted three valued reasoning organisation is able to stand as 0, 1, 2, and -1, 0, 1. This imbalanced three valued reasoning organisation is developed in this work utilising zero point nine five energy source (VDD) besides a ground potential of 0 V. Table 1 shows the convention for instable three valued reasoning ethics besides their accompanying energy stages.

An Over-all Three valued device for supplying the power (GTI) is able to have one of ternary sorts based on its operating principle: Negative, Positive, or Standard. (1), (2), and (3) depict an Adverse three valued device of power supply (NTI), the Optimistic three valued device of power supply (PTI), besides the Regular three valued device of power supply (STI), correspondingly [20], the x is the input and y0, y1, y2 might be outputs.

TABLE I THREE VALUED VOLTAGE LEVEL AND LOGIC LEVELS

Voltage Level	Logic Symbol
0 V	0(Low)
1/2 V_{DD} (0.45V)	1(Intermediate)
V_{DD} (0.9V)	2(High)

TABLE II

GENUINE TABLE OF NTI, PTI & STI

Input(x)	NTI(Y_0)	PTI(Y_1)	STI(Y_2)
0	2	2	2
1	0	2	1
2	0	0	0

Table 2 shows the genuine statistics which are reflecting the functions y0, y1, and y2.

$$y0 = Z0\ (x) = \begin{cases} 2, & x = 0 \\ 0, & x \neq 0 \end{cases} \quad (1)$$

$$y1 = Z1\ (x) = \begin{cases} 2, & x = 2 \\ 0, & x \neq 2 \end{cases} \quad (2)$$

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$y2 = Z2\ (x) = \overline{x} = 2 - x$ (3)

A primary arithmetical process for three valued reasons can be prearranged by (4a) and (4b), where, X, Y = {0, 1, 2} [23]. At this time, + besides • symbols epitomise the NOR and NAND manoeuvres, correspondingly. Table three illustrates the real information of three valued system NAND, besides NOR.

$$\overline{X + Y} = \overline{\max(X, Y)} \quad (4a)$$

$$\overline{X \cdot Y} = \overline{\min(X, Y)} \quad (4b)$$

A. The Importance of Gnrfet

One-atom-thick stratum of carbon particles arranged within the hexagonal framework can be carbon by each of two or more different physical forms in which an element can exist by 4 atomic particles happening for electron orbitals that elections can jump out of, moving into the process, similar like silicon, which is a group 4 element. Carbon atoms establish covalent connections with nearby atoms and exhibit largely non-metallic behaviour owing for the occurrence for four atomic particles at furthest group. It can be found in a variety of without metal structures in nature. Once chemical elements of atoms ready to be organised regarding crystal-like arrangement for organic chemical compound with the molecular formula C_6H_6, hexagonal trinkets, however, numerous allotropes with unusual electrical characteristics emerge. Cylindrical particles which are possessing the rolled-up sheets of single-layer carbon particles and one-atom-thick layer of carbon atoms, these two are the most common allotropes of carbon, and both are being investigated as additional constituents to chemical element with the symbol Si and atomic number 14 inside the semiconductor device networks [28].

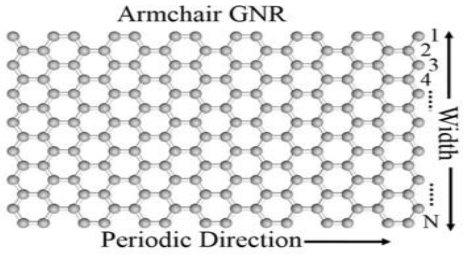

Fig. 1. Size about an Armchair GNR by means of high opinion of Dimer lines.

Reliant arranged at advantage construction, it might either meander or wingchair. Unlike the meander framed GNR, which is continuously copper, this wingchair edged GNR might able to have an electromechanical production value falling between that of a conductor or copper be contingent upon the strip size [29]. Semiconducting GNR would be used in this paper's implemented MVL design[20]–[26].

An organisation with wingchair Graphene Nanoribbon by N Dimer lines is shown in Figure 1. The numeral of dimer lines (N) in a GNR has a significant impact on the GNR's small functioning possessions. When N = 3p or 3p + 1, p with numeral, the GNR shows semiconducting properties [30]– [32]. The breadth of a GNR can might have calculated using

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N likely follows: (5), at the place $a_{c\text{-}c}$ denotes the framework continuous besides the worth is zero point one four two nm.

$$W_{GNR} = (N - 1)\frac{\sqrt{3}}{2} a_{c-c} \qquad (5)$$

MOS-type and Schottky Fence (SB)-type GNRFETs are the dual types with GNRFETs. Schottky fence is existing through metal-graphene boundary in the SB-GNRFET. In its place where the liberation of electrons from an electrode by virtue of its temperature is the kind of insulated-gate field-effect transistor that is invented by the well-ordered oxidation of a semiconductor, characteristically silicon, charge transport is mostly owing to tunnelling phenomena across the barriers. Despite the fact that the tunnelling mechanism can overcome the MOS-type FETs fundamental thermionic limit (60 mV/decade), in SBFET the graphene nano ribbon is used as conducting network and main thing/drain are ready with copper which results in Schottky barrier is preferred aimed at planning three valued reasoning trips due to a number of advantages, including a higher I_{on}-I_{off} proportion owing for the nonappearance with dual glacial transference, advanced Ion, advanced proportion of the modification within power at the end of the productivity to the change in the energy at the end of the contribution which is an active device for improved permeation behaviour because of lesser production functioning, advanced cut-off occurrence, quicker changing rapidity. To improve driving strength and generate a larger contact, multiple parallel ribbons are given. This preparation for the three-strip Graphene nanoribbon is a device which is shown in Figure 2. The channel refers to the segment of the ribbons beneath the gate that is intrinsic in nature. The reservoirs are the portions for the strip that connect the access and the interaction component, additionally they will have extensively fixed by the fixing element with fdop = 0.001 [33]. On picture two, L_{ch} denotes network measurement, L_{res} denotes pool length, W_{ch} (WGNR) denotes ribbon width, W_{gate} denotes gate width, and $2W_{sp}$ denotes ribbon spacing. (6) [33] can be used to calculate the drain current in a GNRFET.

$$I_D(\Psi_{CH}, V_D, V_S) = \frac{2qkT}{h} \sum_{\alpha} \left[\ln\left(1 + e^{\frac{q(\Psi_{CH} - V_S) - \varepsilon_\alpha}{kT}}\right) - \ln\left(1 + e^{\frac{q(\Psi_{CH} - V_S) - \varepsilon_\alpha}{kT}}\right) \right] \qquad (6)$$

Here, Ψ_{CH} = Network probable, V_D = Trough power, V_S = Basis energy, ε_α = Sub band advantage, α = Sub group guide ($1 \leq \alpha \leq N$), k = thermodynamics, Boltzmann continuous is the physical constant relation which is an average kinetic dynamism of the gas atoms and temperature of the gas represented by k or kB, h = the elementary quantum for an action continuously, and T = High temperature. Likely cited previously at the segment, conditionally size regarding GNR may be which similarly numeral with dimer positions (N) stands equivalent to 3p or 3p + 1, which strip demonstrations unique electric conductive behaviour, somewhere between that of a conductor and an insulator. If N = 3p + 2, that strip motivates to have exhibition extra metallic like [32]. Hence, through adjusting worth of N in the GNR network, the verge energy besides Ion-Ioff proportion of the GNRFET is revised at this point for achievement of anticipated multi-valued answer. Table three recapitulates the dependency of the electromechanical possessions for transistor on this numeral of the dimer lines [33].

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Picture three describes t ID vs. Vds curvature in relation through various levels of Vgs. Initially, as Vds rises, the drain current rises in a right pattern, that characterises the rectilinear or the place of a thermionic valve having three electrodes.

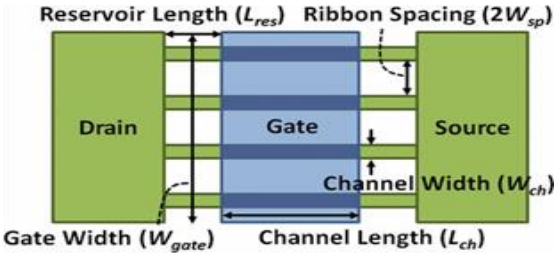

Fig. 2. A three (multiple) ribbon Armchair GNRFET [30].

The current follows a virtually constant value after a given Vds, which marks the saturation region. The ID vs. Vgs curvature with the channel for foundation energy of 1.0 V. The ID vs. Vgs curvature, like any other MOS-transistors, provides a improved indulgent for a verge energy. When Vgs is raised over a certain level, the N-type GNRFET turns on. As the access of energy rises, the power also rises with it. The ID vs. Vgs curvature is shown in Figure for N = 3p, 3p+1, and N = 3p. The GNRFET's with thrice of equivalent fireside chair graphene nano ribbon like a network are employed in all of the simulations in this work. To achieve the desired threshold voltage, a graphene nano-ribbon field effect transistor by varying dimer measurement may be utilized within plan. Each transistor has a channel length of 16 nano meters.

B. Inverter

Figure 3 depicts that of adverse three valued device that supplies the power (NTI) besides optimistic three valued device that supplies a power (PTI) design (PTI). The number of dimmer lines (N) for the p-type and n-type GNRFETs, correspondingly, is 7 and 9. The p-type and n-type GNRFETs have N values of 9 and 7, respectively, for PTI.

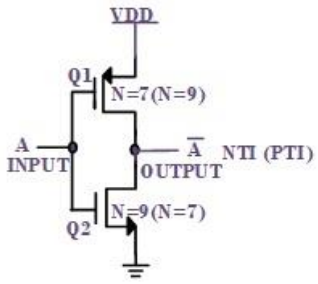

Fig. 3. Representation Illustration of Adverse (Positive) Three valued Device that produce power.

This conventional three valued device of power supplier (STI) architecture is shown in Figure 4. The inverter circuit topology employed at this juncture is comparable towards carbon nanotube field effect transistor may be founded device of power supplier is interconnected has been shown inside [10]. This proposed GNRFET-based ternary inverter, on the other hand, uses a different working value besides methodologies towards production of numerous energy stages. This chirality of the CNTs is adjusted in a CNTFET-based ternary inverter, for example,

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for achievement of dissimilar verge energies. In a GNRFET, at the other side, the width of this graphene nano ribbons is changed to modify the threshold voltage.

The n-type transistors Q1, and Q3 are n-type transistors, while the p-type transistors Q2 is p-type transistors. Q1, Q2, and Q3 have verge energies of -0.24 V, 0.24 V, and 0.6 V, correspondingly. Q1 and Q2 are tuned to N = 7 and Q3 to N = 10 to get the specified threshold voltage. As soon as contribution of power little compared to 0.3 V and it may be increased from low to high, Q1 turn on, resulting in a high output voltage.

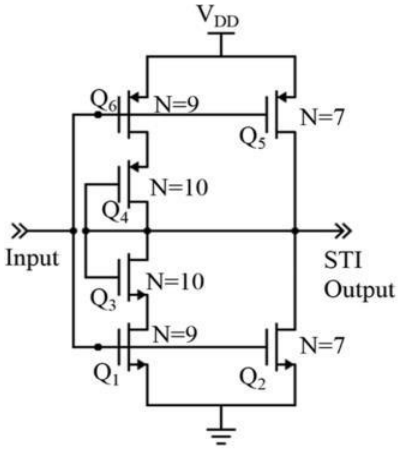

Fig. 4. Representation of Drawing of Normal Three valued Inverter using GNRFET.

Q3 turn at point of time contribution of power may between 0.3 and 0.6 V, Q1 and Q2 turns off. When there is a contribution of energy is between 0.6 V and 0.9 V and is increased from high to low, Q2 turn ON, resulting in a low output voltage.

The momentary answer for more than two times distinct forms of three valued devices is shown in Figure 8. Figure 5 shows the STI's voltage transfer curve, which displays about the device can hold thrice of discrete productivity energy stages over a large variety of contribution energy. The ternary logic circuit is affected by four different noise margins (NM): I noise margin low (NML), (ii) noise margin low-to-medium (NMML), (iii) noise margin medium-to-high (NMMH), and (iv) noise margin high (NMH). The sound boundary study utilising that of transcendental plane curve approach was used to determine the resilience of the more than two distinct energy stages (reasoning positions) about implemented STI, like picture in Figure 6. The transcendental plane bend process may be famous method for calculating this Logic and memory circuit noise margins Figure 6 shows that the STI based on GNRFETs has sufficient sound boundaries towards provide consistent production energies.

C. Ternary Nand and Nor Gates

We designed both three valued NAND besides NOR accesses utilizing similar resolution as the STI. The designs for these gates have been published in the past utilising various technologies [10]. We used GNRFET to implement the designs here. Figure 10 depicts the logic symbol for a ternary NAND gate that has been implemented. The proposal for three valued NOR gate and associated logic symbol are shown in Figure 11. and Figure 12. depicts the ternary NAND and NOR gates transient responses.

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III. PROPOSED STANDARD TERNARY INVERTER

The present segment exhibits an innovative plan of STI and TNAND logic gates as illustrates in Figure 4 and 5.

TABLE III

THIS GENUINE STATISTICS FOR THE THREE TERNARY INVERTERS

Ternary Input	STI	NTI	PTI
Logic 0 (0 V)	2	2	2
Logic 1 (0.45 V)	1	0	2
Logic 2 (0.9 V)	0	0	0

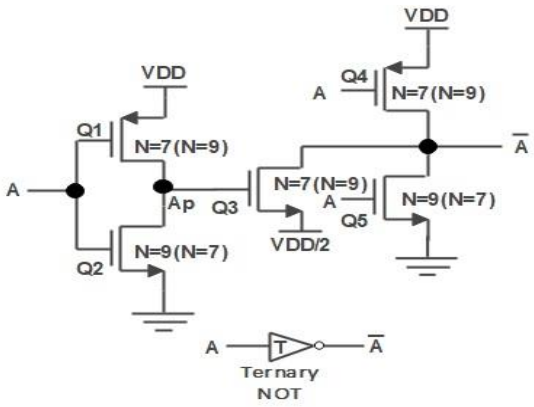

Fig. 5. Proposed Standard Ternary Inverter.

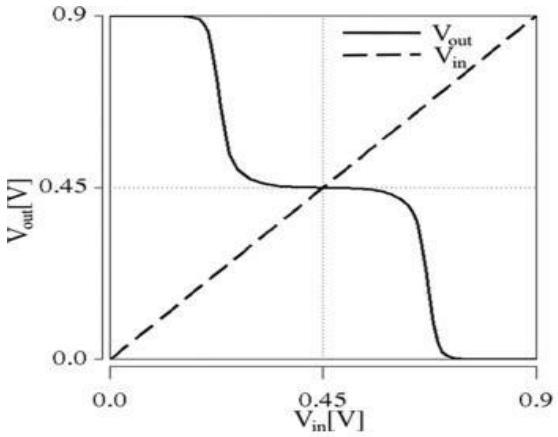

Fig. 6. Transfer curve of STI using GNTFET.

Table 6 posturizes thorough the manoeuvre by the Fig.5 which is proposed STI circuit. The transistors Q1, Q4 AND Q5 are switched on the transistors Q2 AND Q5 are switched off, due to its result will be logic 0 at the time when A is taken into implementation.

When output Ap makes to logic 2, the transistor (Q3) activated. As a result, the outcome equals logic 2. At the time of input A becomes as logic 1, transistor (Q1) is activated, while transistors (Q2, Q4, Q5) deactivated.

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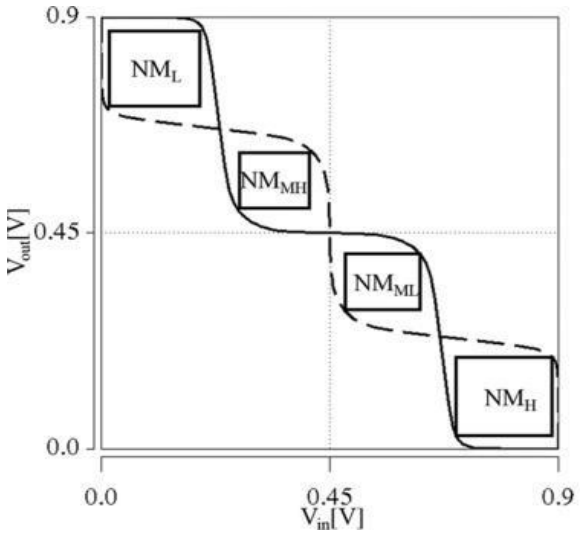

Fig. 7. Noise Margins for GNRFET-based STI are shown as butterfly curves (NM).

When output Ap equals logic 2, the transistor (Q3) is activated. As a result, the output equals logic 1. At the time of input A becomes logic 2, transistors (Q2, Q5) might switched ON, while transistors (Q1, and Q4) are switched OFF. The transistor (Q3) can be switched off when the Ap equals towards logic 0. As a result, the output equals to logic 0.

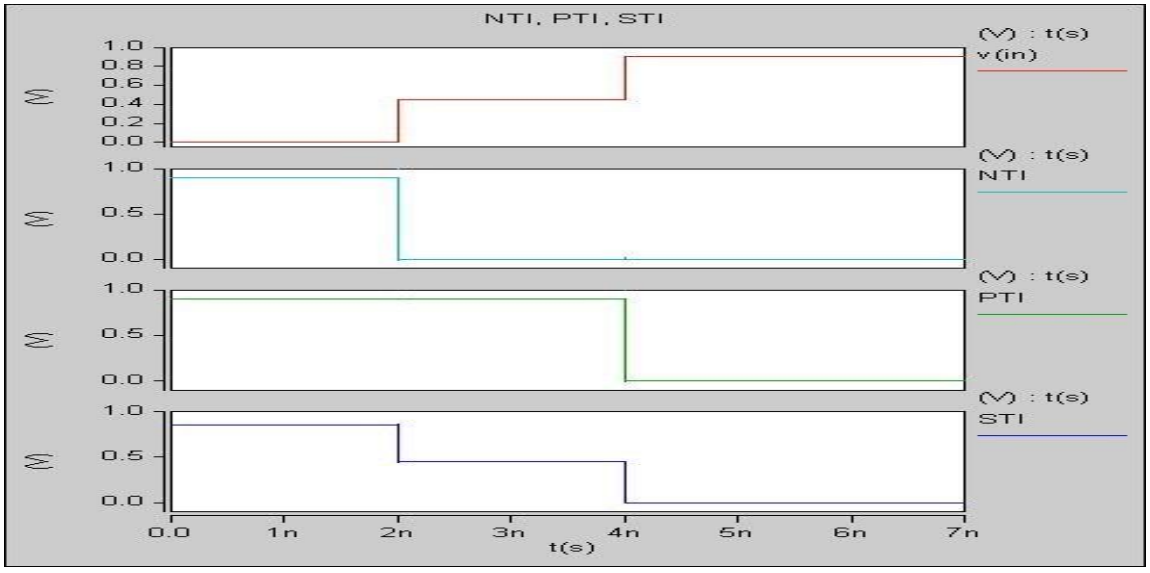

Fig. 8. The proposed transient analysis of STI.

A. Proposed Ternary Nand

Figure. 3 describes this transistor which is designed for two inputs proposed TNAND at the place of dimer line, by the side of threshold voltage (Vth) of the GNRFETs utilized might be exhibited in Table 4.

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TABLE IV THE DIMER LINE, ALSO THRESHOLD VOLTAGE OF GNRFETS UTILIZED IN PROPOSED T NAND AND T NOR.

GNRFET Type	Dimer Line (N)	V_{th}
P-GNRFET (Q1, Q3, Q7, Q8)	7	-0.559
P-GNRFET (Q5, Q6)	6	-0.428
N-GNRFET (Q9, Q10)	7	0.559
N-GNRFET (Q2, Q4)	12	0.289

Table 5 presents the many similarities of the dual ternary inputs A and B that are used for exaggeration of behaviour for expected T NAND gate logic circuit in Figure. 9. Transistors (Q1, Q3, Q7, and Q8) are switched ON at the time of inputs (A, B) are (0 V, 0 V), while transistors (Q2, Q4, Q9, Q10) can be switched OFF. After setting outputs (An, Bn) to (0.9 V, 0.9 V), transistors (Q5, and Q6) can be switched OFF. Hence, this output becomes to 0.9 V. Transistors (Q1, Q4, and Q7) are switched ON at the time of inputs (A, B) can be (0 V, 0.45 V), whereas (Q2, Q3, Q8, Q9, and Q10) are switched OFF. When the outputs (An, Bn) can be equivalent to (0.9 V, 0 V), transistor (Q6) is activated besides it, transistor (Q5) can be deactivated. Hence, the output is equivalent to 0.9 V. Transistors (Q1, Q4, Q7, and Q10) are switched ON at the time of inputs (A, B) are (0 V, 0.9 V) and (Q2, Q3, Q8, and Q9) are turned OFF at the time of the inputs (A, B) can become (0 V, 0.9 V). When outputs (An, Bn) can be equivalent to (0.9 V, 0 V), transistor (Q6) activated besides transistor (Q5) is deactivated. Hence, the output is equivalent to 0.9 V.

At this time of inputs (A, B) become (0.45 V,0 V), at the time of (Q1, Q4, Q7, Q9 and Q10) becomes switched OFF. The Transistors (Q2, Q3 and Q8) are switched ON. When outputs (An, Bn) can be equivalent towards (0 V, 0.9 V), transistors (Q5) and (Q6) are switched OFF and ON, respectively. Hence, output is equivalent to 0.9 V. Transistors (Q2, and Q4) are switched ON at the time of inputs (A, B) becomes (0.45 V, 0.45 V), whereas transistors (Q1, Q3, Q7, Q8, Q9, and Q10) are turned OFF. Transistors (Q5, and Q6) are turned ON once the outputs (An, Bn) can becomes set to (0 V, 0 V). Hence, the output is equals to 0.45 V. At the time of the inputs (A, B) are (0.45 V, 0.9 V), transistors (Q2, Q4, and Q10) are switched ON, while transistors (Q1, Q3, Q7, Q8, and Q9) turn OFF. Transistors (Q5, and Q6) are turned ON once outputs (An, Bn) can be set to (0 V, 0 V). Hence, the output can be equivalent to 0.45 V. At the time of inputs (A, B) are (0.9V, 0V), transistors (Q2, Q3, Q8, and Q9) turn ON, while transistors (Q1, Q4, Q7, and Q10) turn OFF. When the outputs (An, Bn) reach 0 V and 0.9 V, transistor (Q5) is switched ON and transistor (Q6) is switched OFF. Hence, output can be equals to 0.9 V. At time of inputs (A, B) can become (0.9V, 0.45V), transistors (Q2, Q4, Q9) turn ON, whereas transistors (Q1, Q3, Q7, Q8, and Q10) turn OFF. Transistors (Q5, Q6) are turned ON after the outputs (An, Bn) can be equalled to (0.9 V, 0.9 V). Hence, the output is equals to 0.45 V.

Lastly, at the time of the inputs (A, B) are (0.9V, 0.9 V), therefore transistors (Q2, Q4, Q9, Q10) switched ON and transistors (Q1, Q3, Q7, and Q8) switched OFF. These outputs (An,

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Bn) can be equals to (0.9 V, 0.9 V), therefore transistors (Q5, Q6) can becomes switched ON. Hence, output is equivalent to 0 V.

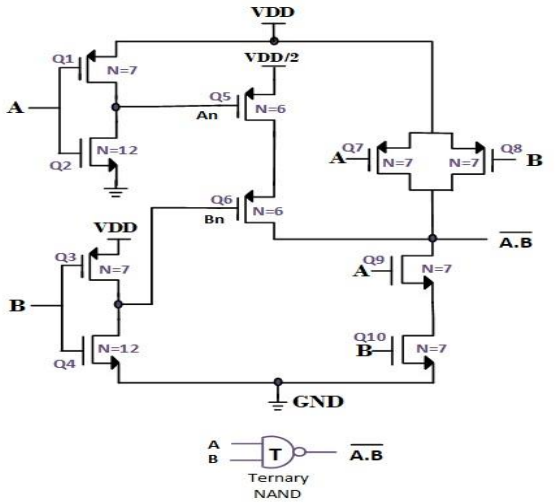

Fig. 9. Transistor Level of this proposed T NAND.

B. Proposed Ternary Nor

Figure 10 illustrates this transistor stage for planning in this anticipated dual inputs TNOR at the place of dimer line, besides threshold voltage (Vth) for GNRFETs utilized to be described in Table 3. Table 6 posturized this particular amalgamations of dual ternary inputs A and B to define this procedure for this anticipated TNOR logic circuit of Figure 10. Transistors (Q1, Q3, Q7, and Q8) are switched ON at the time of inputs (A, B) are (0 V, 0 V), while transistors (Q2, Q4, Q9, and Q10) are switched OFF. After setting the outputs (An, Bn) towards (0.9 V, 0.9 V), transistors (Q5, and Q6) are switched OFF. Hence,

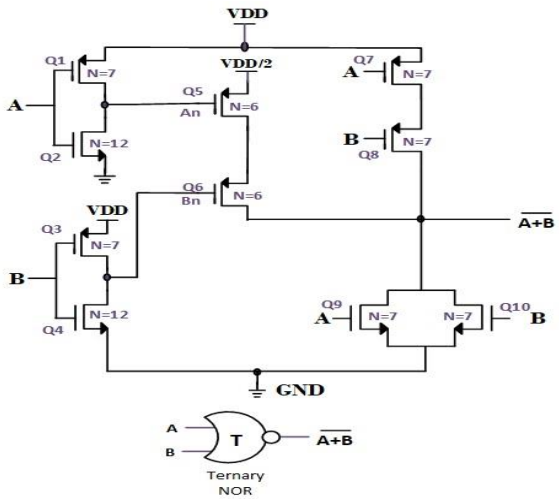

Fig. 10. Transistor Level of the proposed T NOR.

output is equals to 0.9 V. Transistors (Q1, Q4, and Q7) can be switched ON at the time of the inputs (A, B) become (0 V, 0.45 V), whereas (Q2, Q3, Q8, Q9, and Q10) are switched OFF. When outputs (An, Bn) are equivalent to (0.9 V, 0 V), transistor (Q6) can be activated, transistor (Q5) deactivated. Hence, the output equals to 0.9 V.

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Transistors (Q1, Q4, Q7, and Q10) are switched on at the time of the inputs (A, B) can become (0 V, 0.9 V) and (Q2, Q3, Q8, and Q9) are turned OFF at the time of the inputs (A, B) are (0 V, 0.9 V).

TABLE V THE THOROUGH PROCEDURE OF T NAND WITH SELECTED INPUTS OF FIG. 9.

Ternary Inputs (A, B)	**(0, 0)**	**(0, 1)**	**(0, 2)**	**(1, 0)**	**(1, 1)**	**(1, 2)**	**(2, 0)**	**(2, 1)**	**(2, 2)**
P-GNRFET T1	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
N-GNRFET T2	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON
An	2	2	2	0	0	0	0	0	0
P-GNRFET T3	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
N-GNRFET T4	OFF	ON	ON	OFF	ON	ON	OFF	ON	ON
Bn	2	0	0	2	0	0	2	0	0
P-GNRFET T5	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON
P-GNRFET T6	OFF	ON	ON	OFF	ON	OFF	OFF	ON	ON
P-GNRFET T7	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
P-GNRFET T8	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
N-GNTFET T9	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
N-GNTFET T10	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
Output T NAND	2	2	2	2	1	1	2	1	0

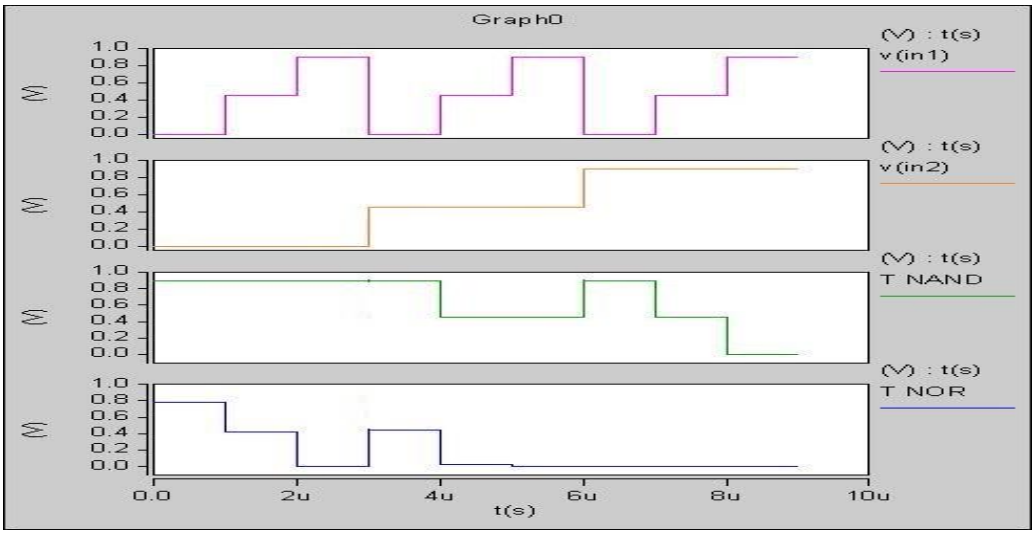

Fig. 11. The proposed transient response of TNAND and TNOR gate.

When outputs (An, Bn) can be equivalent to (0.9 V, 0 V), transistor (Q6) is activated, transistor (Q5) is deactivated. Hence, the output is equivalent to 0 V. Transistors (Q2, Q4, Q7, and Q8) are switched on at the time inputs (A, B) can be (0.45 V, 0 V), while transistors (Q1, Q3, Q9,

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and Q10) might be switched OFF. After setting outputs (An, Bn) to (0.9 V, 0.9 V), transistors (Q5, and Q6) can be switched OFF. Hence, the output is equivalent to 0.45 V. Transistors (Q2, and Q4) are switched ON at the time of inputs (A, B) are (0.45 V, 0.45 V), whereas transistors (Q1, Q3, Q7, Q8, Q9, and Q10) are switched OFF. Transistors (Q5, and Q6) are turned ON once outputs (An, Bn) are set to (0 V, 0 V). Hence, the output is equivalent to 0.45 V. When the inputs (A, B) are (0.45 V, 0.9 V), transistors (Q2, Q4, and Q10) turn ON, whereas transistors (Q1, Q3, Q7, Q8, and Q9) turn OFF. Hence, the output is equivalent to 0 V. At the time of inputs (A, B) might be (0.9V, 0 V), transistors (Q2, Q3, Q5, Q8, and Q9) turn ON, whereas transistors (Q1, Q4, Q6, Q7, and Q10) switch OFF. When the outputs (An, Bn) can be equivalent to 0 V and 0.9 V, the transistors (Q5) and (Q6) are switched ON. Hence, the output is equivalent to 0 V. At time of inputs (A, B) become (0.9V, 0.45 V), transistors (Q2, Q4, and Q9) turn ON, whereas transistors (Q1, Q3, Q7, Q8, and Q10) switch OFF. Transistors (Q5, Q6) are turned ON once the outputs (An, Bn) are set towards (0 V, 0 V). Hence, the output might equivalent to 0 V.

Due to it's consequence, for all these, whenever there are the inputs (A, B) can become (0.9V, 0.9 V), therefore transistors (Q2, Q4, Q9, Q10) are switched ON (Q1, Q3, Q7, and Q8) are switched OFF. The outputs (An, Bn) can be equivalent to (0 V, 0 V), then transistor (Q5, Q6) can be switched

ON. Henceforth, the output might be similar to 0 V.

D. Proposed Ternary Decoder Circuit

The section proposes one of this combinational circuit alike T Decoder.

As exhibited in Figure 12, the section offers an innovative T Decoder architecture with NINE transistors by in the place of the T NOR and second NTI with the new sub-circuit and a binary inverter, respectively. Figure 12 depicts the planned T Decoder's transistor level design.

Ternary decoder with one ternary input (X), and three binary outputs (X0, X1, X2) are illustrated

mathematically in it's equation (7) and these genuine statistics can be exhibited in Table 7.

$$X_k = \begin{cases} 2 & x = k \\ 0 & x \neq k \end{cases} \qquad (7)$$

One negative ternary inverter (NTI), one positive ternary inverter (PTI), one binary inverter, and a new sub-circuit make up this circuit. Table 6 shows the dimer line, threshold voltage (Vth) of GNRFETs employed, and Table 7 describes the thorough procedure of the anticipated circuit. Whenever input X might be a logic 0, transistors (Q1, Q3) and (Q2, Q4, and Q7) are switched ON and transistors (Q2, Q4, and Q7) are switched OFF. The intermediate Y as well as the output X0 are both equivalent to logic 2. Q5 and

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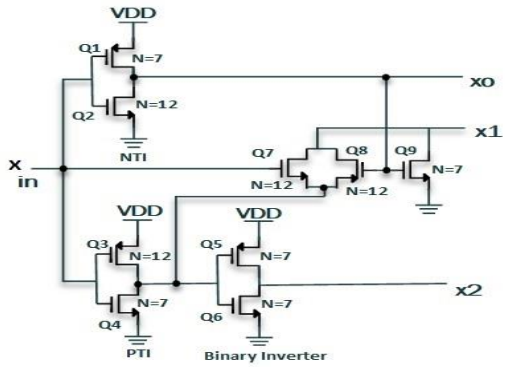

Fig. 12. The proposed transistor Level of T Decoder with 9 GNRFETs.

Q8 are then switched OFF, and Q6, and Q9 are switched ON.

As a result, the X1 and X2 outputs are both logic 0. Whenever might input X is logic 1, transistors (Q2, Q3, and Q7) turn ON, transistors (Q1, and Q4) turn OFF. This intermediate Y can be similar to logic 2, in addition to output X0 is similar to logic 0. Then (Q5, Q9) is switched OFF (Q6, Q8) is switched on. As a result, the output X1 equals the logic 2 value of Y, and the output X2 equals logic 0.

TABLE VI THE THOROUGH MANOEUVRE OF T NOR WITH SELECTED INPUTS OF FIG. 10.

Ternary Inputs (A, B)	**(0, 0)**	**(0, 1)**	**(0, 2)**	**(1, 0)**	**(1, 1)**	**(1, 2)**	**(2, 0)**	**(2, 1)**	**(2, 2)**
P-GNRFET T1	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
N-GNRFET T2	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON
An	2	2	2	0	0	0	0	0	0
P-GNRFET T3	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
N-GNRFET T4	OFF	ON	ON	ON	ON	ON	OFF	ON	ON
Bn	2	0	0	2	0	0	2	0	0
P-GNRFET T5	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON
P-GNRFET T6	OFF	ON	ON	ON	ON	ON	OFF	ON	ON
P-GNRFET T7	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
P-GNRFET T8	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
N-GNTFET T9	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
N-GNTFET T10	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
Output T NAND	2	1	0	1	1	0	0	0	0

As consequent, at time of input X is logic 2, transistors (Q2, Q4, Q7) can be switched ON, while transistors (Q1, Q3) are switched OFF. Logic 0 is equivalent to the output X0 and the intermediate Y. Then (Q6, Q9)

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are switched OFF, followed by (Q5, Q8) being switched ON. As a result, the output X1 equals the logic 0 value of Y, while the output X2 equals logic 2.

TABLE VII THE DIMER LINES, AND THRESHOLD ENERGY OF THE GNRFETS UTILIZED IN THE ANTICIPATED T DECODER

GNRFET Type	Dimer Line (N)	V_{th}
P-GNRFET (Q2, Q5)	7	-0.559
P-GNRFET (Q3, Q8)	12	-0.289
N-GNRFET (Q4, Q6, Q9)	7	0.559
N-GNRFET (Q2, Q7)	12	0.289

TABLE VIII

THE PROPOSED T DECODER DETAILED OPERATION OF FIG. 12.

Ternary Input X	**0 (0 V)**	**1 (0.45 V)**	**2 (0.9 V)**
P-GNRFET T1	ON	OFF	OFF
N-GNRFET T2	OFF	ON	ON
Output X0	**2**	**0**	**0**
P-GNRFET T3	ON	ON	OFF
N-GNRFET T4	OFF	OFF	ON
Intermediate Y	**2**	**2**	**0**
P-GNRFET T5	OFF	OFF	ON
N-GNRFET T6	ON	ON	OFF
Output X2	**0**	**0**	**2**
N-GNRFET T7	OFF	ON	ON
P-GNRFET T8	OFF	ON	ON
N-GNTFET T9	ON	OFF	OFF
Output X1	**0**	**Y=2**	**Y=0**

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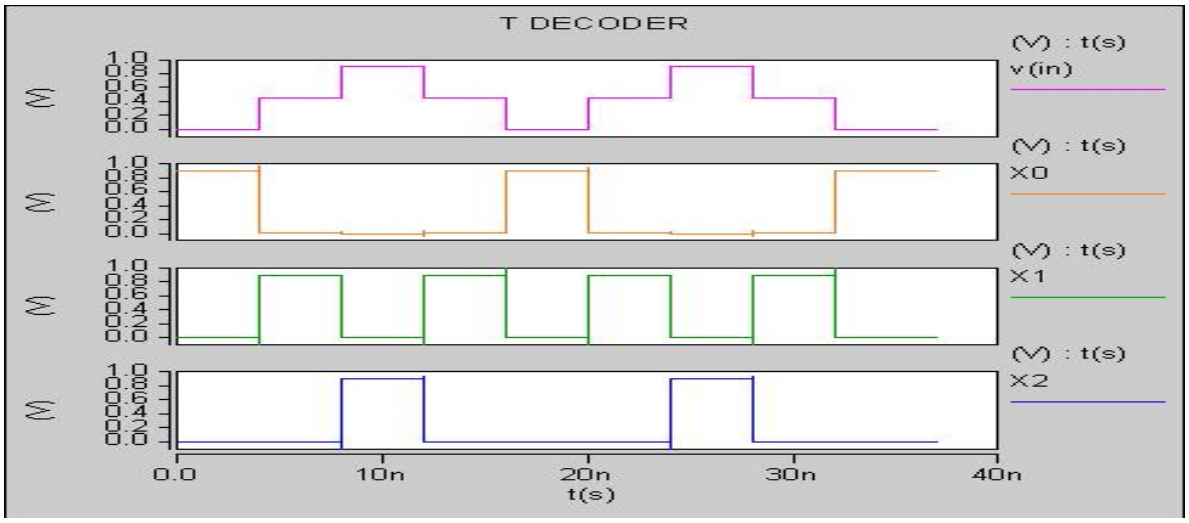

Fig.13. The proposed transient analysis of T Decoder.

TABLE IX COMPARATIVE ANALYSIS BETWEEN THE PROPOSED GNRFET BASED TERNARY LOGIC GATES AND EXISTING CNTFET.

	Logic Gates	Transistor count	Delay (ps)	Total Power (nW)	Power Delay Product (PDP) e^{-18}
STI	CNTFET [34]	6	11	88.6	0.98
	CNTFET [35]	6	18.8	1170	33.2
	GNRFET [37]	6	30	8100	24
	GNRFET [42]	6	13	23.22	0.302
	Proposed Work	**5**	**0.38**	**11042**	**4.19**
NAND	CNTFET [34]	10	3	100.8	0.3
	CNTFET [35]	-	27.6	704.8	19.46
	CNTFET [37]	10	58	1580	92
	GNRFET [42]	10	5.2	27.5	0.14
	Proposed Work	**10**	**1.57**	**4223**	**6.63**
NOR	CNTFET [34]	10	2	100	0.2
	CNTFET [35]	-	27.3	1054	28.79
	GNRFET [37]	10	47	1635	77
	GNRFET [42]	10	3.33	27.42	0.1
	Proposed Work	**10**	**1.38**	**3181**	**4.39**
DECODER	CNTFET [34]	10	3	100.8	0.3
	CNTFET [35]	-	27.6	704.8	19.46
	GNRFET [37]	10	58	1580	92
	GNRFET [42]	10	5.2	27.5	0.14
	Proposed Work	**9**	**4.1**	**88.3**	**0.362**

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IV. COMPARISON

Most of the CNTFET are constructed ternary logic gate access strategies have been discovered in the literature. GNR, rather than CNT, is commonly thought to have a preferable alternate to choose transistor network. As a result, the focus of this research is on the implementation for three value besides mathematical circuits by means of GNRFETs. In a latter part of this section, a comparison of selected one are CNTFET, GNRFET, CMOS, and projected GNRFET founded fundamental ternary logic circuits is summarised. All simulations are performed using a 50ps input slew and a 1pf output load.

For all of the transistors, the doping fraction f_{dop} is set at 0.001. [13] uses the CNTFET model file from [37] for the simulations. The 16 nm CNTFET transistors utilized in [34] are the CNTFET ideal ones. Figure 14 shows the delay comparison of STI, TNAND, TNOR and TDECODER. Table 9 compares the performance of CNTFET and GNRFET elementary accesses in standings of latency, Leakage Power, Total Power, and Power-Delay-Product (PDP). Our suggested logic

gates show a huge proportion of potential in the realm of three valued strategies in terms of delay, total power, and PDP, as shown in the Table 9.

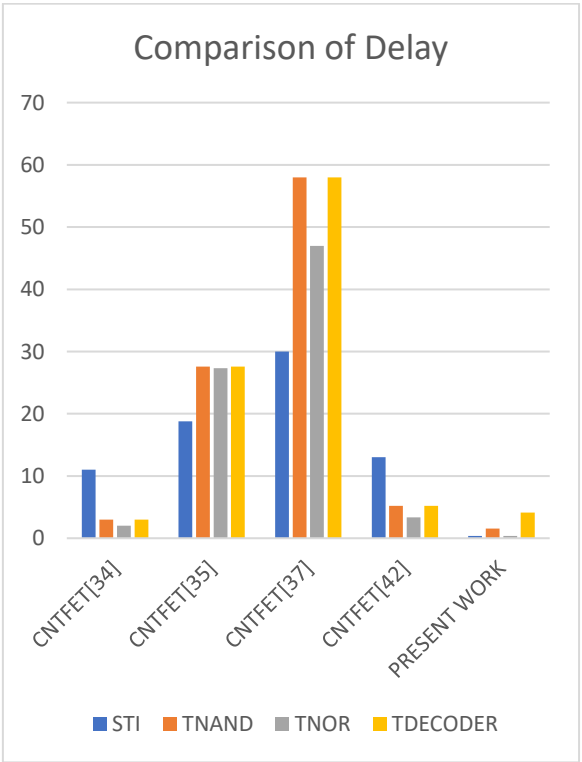

Fig. 14. The comparative transient analysis of Delay.

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V. CONCLUSION

The present study proposes novel proposals for the Standard Ternary Inverter, Ternary NAND, Ternary NOR and Ternary Decoder, all of which are aimed at maintaining excellent performance and energy economy. Several circuit strategies were optimised during the design process, including lowering the amount of employed transistors, using worth full power transistor layouts, besides using twofold source voltages (Vdd and Vdd/2). Any complicated logic, arithmetic, or signal processing circuit can be implemented using these basic gates and circuit.

The basic idea is to change the size of the GNRs to get varied productivity stages while controlling the verge energy and other electrical features of GNRFETs.

Regarding position of postponement, escaping energy, entire power, and power-delay-product, a comparison might be made amid of the proposed GNRFET-based three valued reasoning accesses and courses and present designs (PDP). When matched to familiar accesses and courses founded on CMOS and CNTFET skills, this anticipated GNRFET-founded three valued accesses and circuits provide much improved consequences. The H-SPICE replication and study are carried out utilizing a GNRFET ideal one from Nanohub, with a channel length of 16 nm for the manoeuvre. As a result, the proposed circuits can be used to reduce battery usage in low-power portable devices and embedded systems.

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