

**A COMPREHENSIVE SURVEY ON ANALOG FRONT-END CIRCUITS IN
DIGITAL CONVERTERS WITH EMPHASIS ON BIOMEDICAL SENSOR
APPLICATIONS**

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Abstract

The standard of healthcare services is now being improved via biomedical applications, which are the focus of most technology progress. Since most biomedical equipment is rechargeable and portable, energy-efficient execution is required for all designs. Since analogue signals are the foundation of all communication, digital advancements can only occur when analogue signals can be converted into digital ones. In most biomedical devices, the analog-to-digital converter (ADC) is an essential component. Therefore, this review undergoes analogue front-end design (AFE) for biomedical sensor applications, and the design includes several modules, namely, amplifiers, filters, and ADC modules. This review highlights delta-sigma modulator (DSM) based ADC designs and Successive approximation registers (SAR) based ADC designs for biomedical sensor applications. Additionally, schematic views are provided for the three main ADC design building blocks: the comparator, the digital-to-analogue converter (DAC), and the sample and hold (S/H) circuit. In addition to this, the review undergoes several AFE designs, namely, Low-Noise Amplifier (LNA) and Programmable gain amplifier (PGA) Variable Gain Amplifier (VGA) for biomedical applications with diagrammatic representations. Numerous ADC design and amplifier parameters are eventually addressed in tabular form for improved comprehension. In addition to this, the challenges and future directions are discussed.

Keywords: Analog front end, delta-sigma modulation, successive approximation, comparator, amplifier, biomedical.

1. Introduction

The analog-to-digital converter (ADC) is a recently developed architecture that is widely used in biological applications [1]. The importance of power consumption has drawn more attention in recent years to the design of high-gain integrated circuits. The difficulty of creating new, high-performance analogue circuitry has increased, and this has led to a significant issue with lower supply voltages [2]. Effective wearable sensors are needed for biomedical applications. Compactness is the main factor for biomedical devices, and higher performance also depends on energy efficiency. The need to develop methods for identifying and diagnosing diseases has increased due to the growing pressure on healthcare and medical systems [3]. The medical field is home to the most significant applications, such as wireless sensors and medical implants [4-5]. The wireless body area sensor network (WBSN) design is depicted in Figure 1 [6]. Recently, delta modulators (DM) have been widely utilized in biomedical applications. Further structures are built using level-crossing (LC) delta-modulated ADCs [7]. The sequential approximation register (SAR) ADC has received a lot of interest in recent years. Therefore, SAR ADC is also a suitable option for converting an analogue signal to digital data with regard to low power issues [8-12].

An analogue front-end (AFE) typically includes an amplifier, appropriate filtering, and an ADC to connect with the sensor. In a current-sensing AFE, a trans-impedance amplifier (TIA) and a current-to-frequency converter convert the sensor output to voltage and time, respectively. Classifying and identifying patients based on biological signals can help with the rapid diagnosis of relevant illnesses and the delivery of essential medical care [13, 14]. Converting signals from one kind to another is the third function of AFEs. The majority of analogue signal transducers, such as instrumentation bio amplifiers, pressure sensors, and analogue accelerometers. etc., produce both voltage and current as output [15, 16]. Several types of ADC (DSM, SAR) included in AFEs are unable to process with current inputs. Therefore, the voltage conversion is necessary before sending the voltage to the ADC input. A separate AFE unit called a transimpedance converter (current-to-voltage) performs this conversion of current to voltage and amplifies the resulting voltage to the required level. To remove an undesired component, the low pass filter is essential, and it takes place between the front-end amplifier and ADC.

There are several difficulties in designing CMOS-based AFE circuits for biomedical applications, especially in noninvasive physiological monitoring. Recent works, such as Ha et al. [79], have explored integrated circuits and electrode interfaces that enable high-fidelity biosignal acquisition. For long-term monitoring, controlling electrode-skin impedance, minimizing motion artifacts, and maximizing power usage are important factors. The efficiency of biomedical AFEs is largely determined by the trade-offs between power, noise, and signal integrity, which calls for sophisticated circuit design strategies, including chopper modulation, impedance tracking, and energy-efficient biasing.

One of the most important biological data acquisition methods is electrocardiography (ECG), which is widely used to diagnose cardiac disorders like arrhythmias, myocardial infarctions, and heart rate variability. The performance of the AFE circuits, analyzing weak bioelectrical signals while reducing noise, power consumption, and interference, is crucial to the effectiveness and precision of ECG monitoring systems. The effectiveness of the AFE circuit handles weak bioelectrical data while reducing noise and power consumption, which is a critical component of an ECG-based monitoring system. The main focus of this review is on AFE circuit topologies specifically designed for the acquisition of ECG signals by addressing important design factors, including power-efficient analog-to-digital conversion, programmable gain control, and low-noise amplification. The circuits under review are designed to record high-fidelity ECG signals as well as other biological data that are pertinent to the analysis of cardiac parameters. With an emphasis on their efficacy in cardiac signal processing, the review also classifies AFE circuit topologies according to their amplifier architectures, filtering strategies, and ADC implementations. Through this work, researchers examine new trends in next-generation low-power, high-precision biomedical AFE systems, emphasize the development of ECG-specific AFE circuits, and pinpoint important design trade-offs. The framework of biomedical acquisition is illustrated in Figure 2.

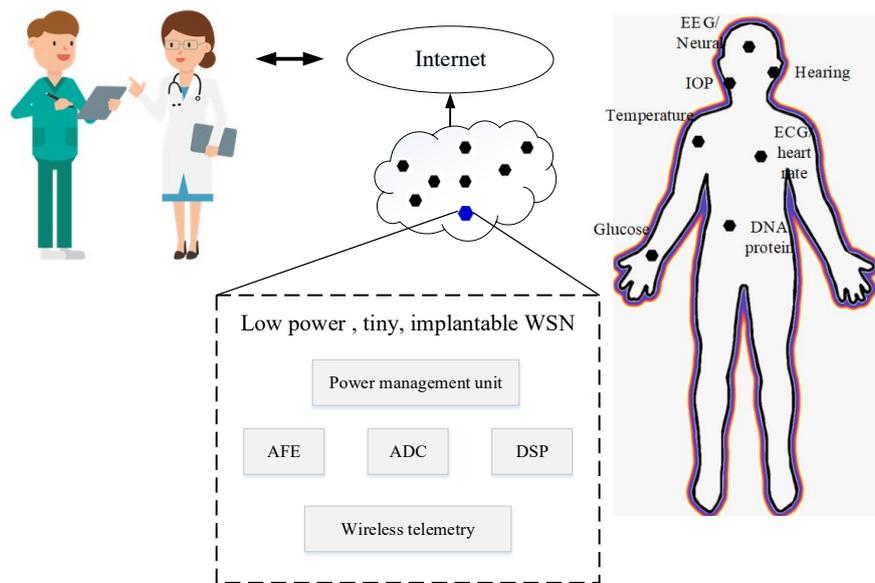


Figure 1: Architecture of WBSN

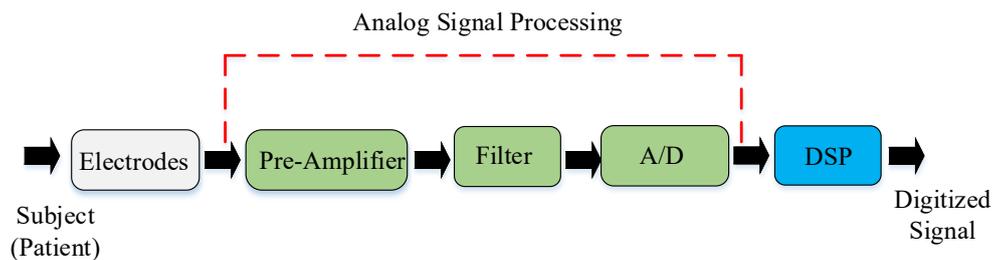


Figure 2: Framework of biomedical signal acquisition

The yearly distribution of research articles for CMOS analog front-end circuits for biomedical applications is shown in Figure 3. This information has been gathered to demonstrate the ten-year increase in interest in this field. With an emphasis on low power consumption, high signal quality, and effective data conversion methods, the increasing number of publications reflects the quick developments and research efforts devoted to enhancing AFE circuit designs. The pattern illustrates how advancements in amplifiers, filters, and ADC architectures have improved signal capture and processing, highlighting the technological development of biomedical sensor interfaces.

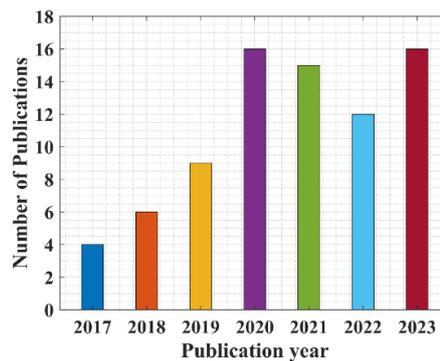


Figure 3: Annual distribution of research publications related to CMOS analog front-end circuits for biomedical applications. The increasing number of studies highlights the growing research interest and technological advancements in this field.

There have been a lot of studies on biomedical sensor ADC design, but there hasn't been a thorough analysis that compares the trade-offs between SAR-ADC and Delta-Sigma designs. The majority of assessments that presently exist focus on the individual circuit components rather than how well they work together in biological applications. In order to close this gap, this review evaluates ADC architectures in light of practical biomedical requirements such as high signal quality, noise efficiency, and low power consumption.

1.1 Review Methodology

CMOS-based AFE circuits for biomedical applications were reviewed thoroughly and methodically using a well-defined literature selection approach. Using the following methodology, the research publications were chosen based on their impact, relevance, and recentness:

1.1.1 Database Sources

The literature review was conducted by searching reputable academic databases, including:

- IEEE Xplore
- PubMed
- ScienceDirect
- SpringerLink
- Google Scholar

These sources were selected because of their vast collection of technical reports, conference proceedings, and peer-reviewed journal publications about analog circuit design and biomedical electronics.

1.1.2 Search Keywords and Criteria

To extract the most relevant studies, the following keyword combinations were used:

- "CMOS analog front-end for biomedical sensors"
- "Low-power AFE design for ECG and EEG acquisition"
- "Biomedical ADC architecture: DSM and SAR approaches"
- "Instrumentation amplifiers for biosignal acquisition"
- "Power-efficient signal processing in biomedical sensors"

Search results were filtered using boolean operators (AND, OR) to find research papers that particularly addressed the difficulties and developments in AFE circuit designs for biomedical applications.

1.1.3 Inclusion and Exclusion Criteria

The selected publications adhered to the following criteria:

- **Inclusion Criteria:**
 - Peer-reviewed journal and conference papers from the last ten years (2013–2023).
 - Studies focusing on low-power and high-precision AFE circuits.
 - Research presenting experimental results and performance evaluations of ADCs, amplifiers, and filters.
- **Exclusion Criteria:**
 - Articles with purely theoretical models lacking experimental validation.
 - Studies focus solely on digital signal processing without discussing AFE hardware.
 - Patents and non-peer-reviewed articles.

A comprehensive assessment of current trends, design difficulties, and possible future directions for AFE circuits in biomedical applications is provided by this methodical selection process, which guarantees that the review includes the most important contributions in the field.

1.2 Classification and Evaluation of AFE Circuits

The selected works were categorized based on circuit architecture, performance trade-offs, and target applications. The classification was structured as follows:

- ***Low-Noise Amplifier (LNA) Designs:*** Techniques such as chopper stabilization, capacitive feedback, and subthreshold operation were evaluated based on their noise efficiency and common-mode rejection ratio (CMRR).

- **Filtering and Signal Conditioning Blocks:** Various high-pass and low-pass filter designs were analyzed, considering their bandwidth tuning ability and power constraints.
- **Data Conversion Techniques (ADC Architectures):** Successive Approximation Register (SAR) ADCs, Delta-Sigma Modulators (DSM), and Pipeline ADCs were examined in terms of power efficiency, resolution, and suitability for biomedical signal processing.

A comparative evaluation of these circuit topologies was conducted by linking design choices with key performance metrics such as power consumption, noise figure, linearity (THD), bandwidth, and gain accuracy.

2. Motivation and Summary of Review

The development of several healthcare applications, from wearable technology for continuous health monitoring to advanced diagnostic tools, has been greatly impacted by the quick evolution of biomedical sensor technology. These sensors need to function reliably in a variety of conditions with high precision and low power consumption. The AFE design is critical to defining the overall performance of the biomedical sensor systems in order to achieve these high requirements. To identify weak bio-signals, such as electrocardiograms (ECG), electroencephalograms (EEG), and other physiological signals, biomedical sensors need to have a high degree of accuracy and sensitivity. These signals need to be filtered and amplified by the AFE without any noise or distortion.

For biomedical sensor systems, the process of transforming analogue bio signals to digital form is essential. The choice of ADC architecture significantly impacts the accuracy and reliability of the data. This review is motivated by the evaluation of a detailed analysis of various ADC designs, including successive approximation registers (SAR) and delta-sigma modulators (DSM), which are renowned for their energy efficiency and fit for small, low-power applications. The designs are essential for producing digital data with low power consumption and good resolution from analog bio-signals. These ADCs are essential in situations where power efficiency and data integrity are crucial.

Along with useful schematic representations, the review attempts to offer educational insights into the essential components of ADC design, such as the comparator, DAC, and sample and hold (S/H) circuit. For precise signal processing, low-noise amplifiers (LNA) are necessary to reduce the noise generated during signal acquisition. The review highlights the significance of LNA designs for improving signal integrity as they relate to biomedical applications. Variable gain amplifiers (VGA) and programmable gain amplifiers (PGA) are covered in this review because they offer the flexibility required to adjust for various signal intensities. In biomedical applications, where signal amplitudes can fluctuate greatly, this flexibility is essential. To prevent loading effects and preserve signal integrity, amplifiers with high input impedance are particularly important in designs such as VGA and PGA. Novel circuit designs that improve impedance without sacrificing other performance metrics might be the focus of these types of breakthroughs. A comprehensive review that covers different AFE design methodologies, such as amplifiers, filters, and ADC modules, is necessary due to the diverse requirements of biomedical sensor applications.

This review provides a comprehensive resource for researchers and technologists working on the development of high-performance biomedical sensors. This will help researchers to understand the complex design factors required to create reliable biomedical sensors. The overall goal of this review is to bridge the knowledge gap between the theoretical basis of AFE design and their real-world applications in biomedical sensor systems. This review attempts to guide future advancements in the sector and ultimately aid in the development of more dependable and efficient biomedical equipment by offering comprehensive insights into the design considerations and challenges.

2.1 Research contribution

- **Comprehensive Analysis of CMOS-Based AFE Architectures:** A thorough analysis of several CMOS-based AFE architectures designed especially for ECG signal capture is reviewed in this article. This study offers an integrated viewpoint, examining the function of amplifiers, filters, and ADCs in a single framework for biomedical applications, in contrast to earlier assessments that concentrate on specific circuit components.
- **Parametric Comparison and Performance Trade-Offs:** A unique contribution of this study is the comparative evaluation of key performance parameters, including power consumption, noise efficiency, dynamic range, common-mode rejection ratio (CMRR), and linearity. The trade-offs between different AFE circuit topologies are systematically analyzed, providing valuable insights into their suitability for wearable and implantable medical devices.
- **Advancements in Delta-Sigma and SAR ADC Architectures:** This review focuses on the transition from traditional ADC architectures to optimized designs that improve signal resolution and power efficiency. Special emphasis is placed on hybrid ADC topologies, which integrate the benefits of the Successive Approximation Register (SAR) and Delta-Sigma Modulation (DSM) for low-power, high-precision biosignal acquisition.
- **ECG-Specific Circuit Innovations and Interference Mitigation:** Unlike general-purpose AFE designs, this work specifically addresses challenges in ECG signal acquisition, such as motion artifacts, baseline wander, and power-line interference. The study discusses chopper-stabilized amplifiers, adaptive filtering techniques, and dynamic biasing strategies that improve ECG signal integrity in real-world biomedical applications.
- **Incorporation of Advanced AFE Design Techniques:** The study explores the impact of current-mode signal processing, subthreshold analog design, and energy-efficient biasing techniques on next-generation AFE circuits. It also highlights emerging trends such as AI-assisted AFE optimization and machine-learning-based calibration for biomedical electronics.
- **Schematic Representations and Circuit-Level Insights:** Unlike previous literature that provides only theoretical discussions, this study includes schematic diagrams of critical AFE components, such as comparators, DACs, sample-and-hold circuits, and programmable gain amplifiers (PGAs). These schematics enhance the understanding of circuit integration for researchers and engineers working on biomedical sensor front-ends.

- **Trend Analysis and Future Research Directions:** A quantitative analysis of CMOS-based AFE research trends is presented, illustrating the evolution of power-efficient circuit architectures and low-noise amplifier topologies over the past decade. Additionally, the study identifies key research gaps and suggests future directions, including multi-modal sensor fusion, neuromorphic processing for biosignal analysis, and ultra-low-power bioelectronic interfaces.

The review paper is structured as follows: Section 3 describes the ECG generalization framework with several sensor types. Section 4 describes the basics of AFE designs. The ADC design, with its essential modules for medical applications, is described in Section 5, Sections 6 and 7, surveys DSM and SAR designs. Section 8 defines the amplifier designs such as LNA, PGA, and VGA for biomedical applications. Section 9 describes the justification for ADC and amplifiers, and Section 10 describes the parametric analysis. Section 11 discusses the overall work. Section 12 reveals the challenges and future scope. Finally, the review paper ends with the conclusion of section 11.

3. Generalized Framework of ECG

An essential component of cardiac health monitoring is the acquisition of ECG assessments, which calls for extremely sensitive AFE circuits to record, amplify, and digitize bioelectrical signals. These signals, typically in the range of 0.5–5 mV with frequencies between 0.05–250 Hz, demand low-noise, high-gain, and high CMRR amplifier designs to ensure accurate detection. This section examines AFE circuit topologies that are most suited for ECG monitoring, such as active filters, chopper-stabilized instrumentation amplifiers, low-noise amplifiers (LNAs), and ADC modules. These elements are essential for accurately extracting ECG waveforms and related cardiac parameters because they eliminate motion artifacts, minimize common-mode interference, and preserve high signal integrity. The AFE topologies reviewed here are specifically tailored for wearable ECG systems, remote cardiac monitoring devices, and implantable biomedical sensors, highlighting advancements in low-power, high-precision biomedical electronics.

An electrophysiological measurement technique that is frequently used to measure, record, and then analyze electrical potentials that circulate through the heart is called ECG. Research on electrophysiology is essential for the diagnosis of numerous bodily systems. The generalized framework of ECG is illustrated in Figure 4. To ensure data transfer, ECG equipment with Wi-Fi connectivity may be employed [17]. An aggregated ECG from numerous handheld devices can be transported to a central server to gain access to the ECG tracings. The cardiologist can instantly analyze a patient's ECG signal by accessing it through the patient's smartphone or server for classification.

Sensors, IA, and filtering circuits are all included in the AFE design before additional processing can be done. The majority of these components would be included in any ECG signal system, along with optional components like operational and isolation amplifiers. Using the first stage of the IA, any incoming signal is typically amplified to the required amplitude level for simple acquisition [18].

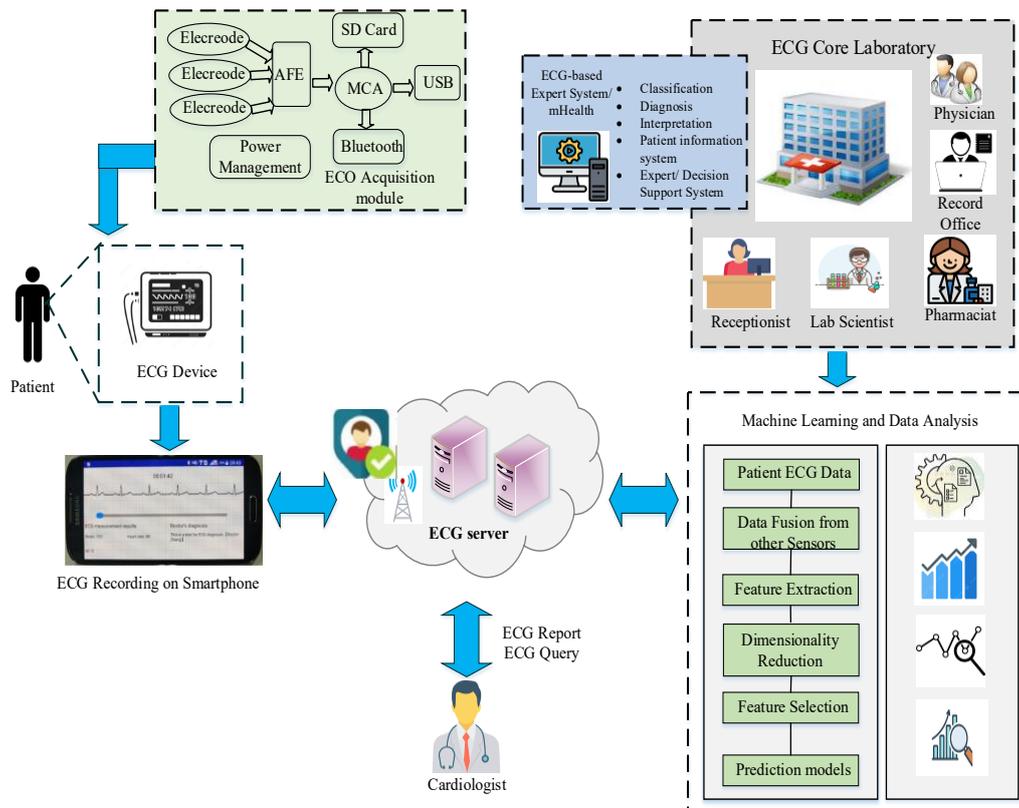


Figure 4: Generalized framework of ECG

3.1 Signal Acquisition Modules

This section discusses the sensor platforms used by various researchers. The process of data gathering, which includes the numerous types of sensors, sensor location, and the equipment required for data collection, storage, and transmission, is the first phase/procedure in the lifespan of ECG monitoring devices. This data gathering technique makes available a variety of sensing platforms and equipment, including ECG electrodes, Internet of Things (IoT) sensors, WBAN sensors, mobile sensors, and wearable sensors. A few examples of sensors and embedded sensors attached to biological tissues that can differ from sensors are smart vests and user-friendly smart watches [19, 20]. Table 1 lists the advantages and disadvantages of signal acquisition modules.

Table 1: Benefits and shortcomings of signal acquisition module sensors

Reference	Sensor types	Advantages	Research gaps
[21]	IoT sensors	Enhanced security and additional features offered by the IoT cloud server, including mobile applications and internet-based monitoring, etc.	Less thorough diagnosis, fewer leads, vulnerability to cyber-attacks, etc.

[22]	WBAN sensors	Portability, excellent linearity and jitter, expandable battery life, low power consumption, etc.	Increased signal delays and ineffective motion artefact reduction.
[23]	Wearable Sensors	reduced power usage, improved and stable input signal impedance, etc.	Increased susceptibility to motion artefacts and customer annoyance.
[24]	Mobile sensors	Low cost, real-time bio-parameter tracking, improved mobility, etc.	It is a less accurate diagnostic and simply records one lead at a time.

3.2 Electrode Interface and Signal Acquisition Challenges

In order to get bioelectric data such as ECG and EEG for noninvasive physiological monitoring, reliable and strong electrode interfaces are necessary. However, there are other obstacles, including motion artifacts, ambient interference, and differences in electrode-skin impedance. To get over these problems, Ha et al. [79] highlight the value of capacitive coupling and dry electrodes. While they are more durable than conventional wet electrodes, dry electrodes have higher impedance and are more susceptible to noise. Chopper-stabilized amplifiers and impedance tracking methods have been suggested as solutions to these problems. Signal fidelity in biomedical applications is enhanced by chopper modulation, which efficiently reduces DC offset and low-frequency noise. The incorporation of impedance adaption circuits improves resilience to motion artifacts, which makes these methods especially appropriate for wearing medical equipment.

4. AFE for Biomedical Sensor Application

The AFE designs, which incorporate various blocks, are listed below:

- The incoming analogue signal must be converted and pre-processed using analogue elements (operational amplifiers, comparators, filters, etc.).
- ADC and DAC converters
- A digital interface for data transmission and system control;
- Power subsystem.

Each of these building blocks is assembled in a particular way to maximize input signal processing efficiency and minimize power consumption. According to the application, the AFE itself executes a variety of tasks. The first AFE function amplifies signals that are too tiny to be handled digitally. Typically, operational, differential, or instrumentation amplifiers are employed for this, and the power needed varies substantially depending on the required performance [25].

4.1 Power-Efficient Circuit Design for Wearable Biomedical Systems

Power efficiency is an important consideration in the design of biomedical AFEs, particularly for wearable and battery-operated monitoring systems. Extremely low power consumption while preserving excellent signal fidelity is crucial, according to Ha et al. [79]. Techniques such as duty cycling, subthreshold operation, and low-leakage biasing have been investigated to reduce energy usage. In particular, duty cycling significantly reduces average power consumption by activating the AFE only during essential signal acquisition periods. Energy-efficient biasing and chopper stabilization work together to reduce low-frequency noise without consuming large amounts of power. Such strategies are essential for the development of next-generation biomedical AFEs that support long-term, continuous physiological monitoring.

Depending on the properties of the sensor, the structure of the AFE amplifier changes [26, 27]. The AFE also has the ability to isolate useful frequency ranges and filter unwanted noise. All of this noise must be removed before the analogue signal can be converted to a digital one. AFE chips often include blocks of analogue low-pass (with anti-aliasing), high-pass, and rejection filters. This is assuming that digital noise filtering at 50–60 Hz will be used [28–30].

The AFE circuit is the most critical in any health monitoring system. After the sensors collect biosignals, the AFE amplifies the weak biopotentials while dampening out-of-band noise. The next step is digitization via an ADC for communications and digital signal processing (DSP). The illustration of AFE and sensor representation are illustrated in Figure 5.

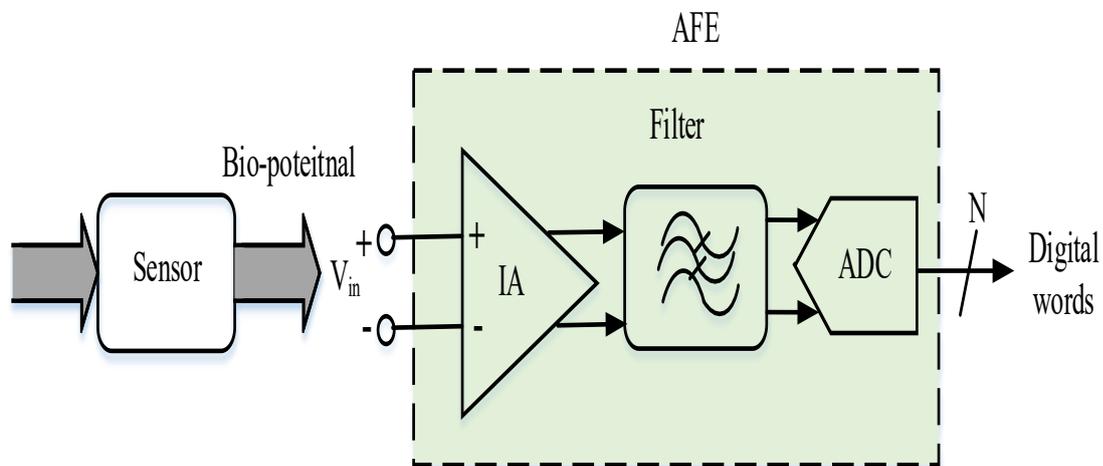


Figure 5: Block diagram of AFE with biomedical sensor application

5. ADC in Biomedical Sensor Application

The ADC structure was built with a variety of circuit topologies, including sample and hold (S/H) switching circuits, dynamic comparator (DC), internal DAC, and SAR control logic. Figure 6 depicts the SAR ADC's fundamental block diagram. As this paper will show, there are numerous ways to reduce power usage.

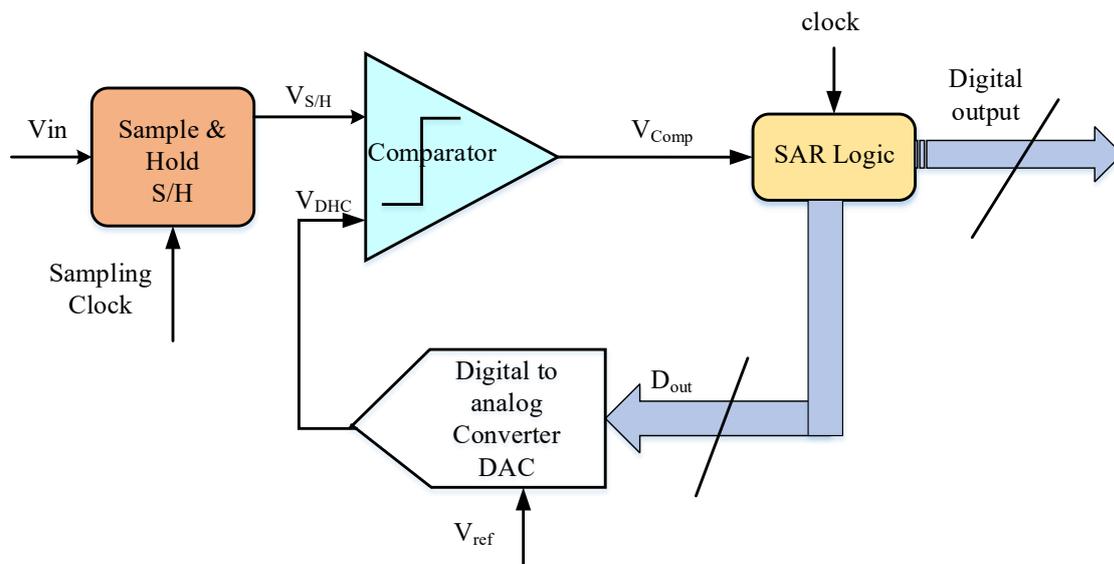


Figure 6: Basic illustration of SAR ADC architectures

5.1 Sample and Hold Circuit

To prevent an aliasing effect, the sampling frequency corresponds to the Nyquist theorem. Using a bootstrap switch is an effective way to increase linearity and reduce power consumption. The traditional bootstrapped S/H circuit is shown in Figure 7, and a comparison between S/H structures is shown in Table 2. A twofold bootstrap switch achieves higher linearity and increased common mode noise immunity [31, 32]. This method supports the SAR comparator's completely differential architecture. It is evident from the comparison that CMOS transmission gates can produce incredibly low power consumption [33]. However, the findings for dynamic linearity and noise are much lower. By using the bootstrap switch, the required specifications will be obtained. The double bootstrap switch method is followed by a dummy switch scheme [34], which uses more power but improves linearity and noise.

Table 2: Comparison between different S/H structures

Structure	CMOS transmission gates	Bootstrap switch	Double bootstrap Switch	Bootstrap switch followed by a dummy switch
Dynamic linearity	Poor	Good	Very low	High
Power consumption	Very low	Low	High	Average
Common mode noise immunity	Low	Average	High	High
Charge injection and clock feed through distortion	High	Average	Low	Very low

5.3 Digital to Analog Converter (DAC)

The growing use of DAC in a variety of biological applications has highlighted the need to reduce power consumption. Multiple capacitive digital audio converter approaches have resulted in a significant reduction in energy usage. The CDAC array structure method, one capacitor splitting method, hybrid redistribution method, and special capacitor array layout method are the four major approaches for distributing the capacitive DAC (CDAC) array. Using several reference voltages also aids in power consumption [37, 38]. Conventional Capacitive DACs are appropriate for low-power applications because of their power efficiency, especially in charge-redistribution systems.

Additionally, it uses binary-weighted capacitors to achieve great resolution with a relatively basic architecture. It is possible to match the capacitors accurately during the fabrication process, which improves linearity and lowers error in the analog output. Comparing capacitive DACs to resistor-based DACs, the latter may be more area-efficient. However, due to their sensitivity to temperature fluctuations, capacitors may cause the output signal to drift. Additionally, the parasitic capacitance might introduce undesirable effects such as charge sharing and coupling, which may affect the accuracy of DAC. Subarray capacitor designs use charge redistribution techniques, which lessen the requirement for constant current flow and make them frequently more power-efficient than standard DACs. Matching and linearity can be enhanced by splitting the capacitor array into subarrays, particularly in designs where the capacitor size is designed for less mismatch.

Capacitor arrays with more compact scaling can be used in these devices to attain better resolution more effectively. Subarray capacitor DACs are appropriate for high-speed applications because of their smaller parasitic capacitance, which allows them to function at higher rates. Compared to traditional designs, these DACs can achieve the required resolution with less silicon area by employing a hierarchical structure with capacitor subarrays. Nevertheless, noise may be introduced by the charge redistribution process in subarray capacitor DACs and potentially lessen the signal-to-noise ratio (SNR) if it is handled improperly. These DACs are more susceptible to mismatched capacitors, which can cause non-linearity and degrade the overall performance of the system. To resolve this, more sophisticated calibrating methods might be required. Overall, the subarray capacitor DAC designs are generally faster, more power-efficient, and able to reach higher resolution with less space. Still, they also demand higher costs, are more difficult to build, and are mismatch-sensitive. The traditional CDAC and subarray capacitor designs are illustrated in Figures 9 and 10, respectively.

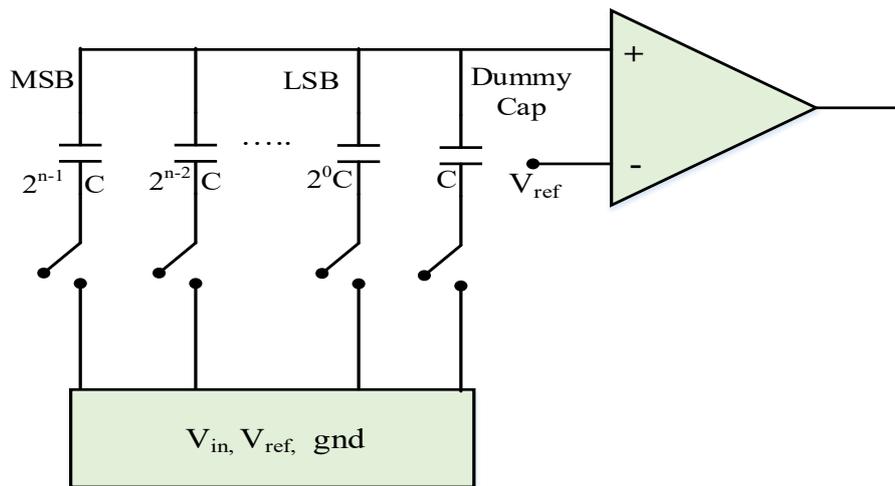


Figure 9: Traditional capacitive DAC

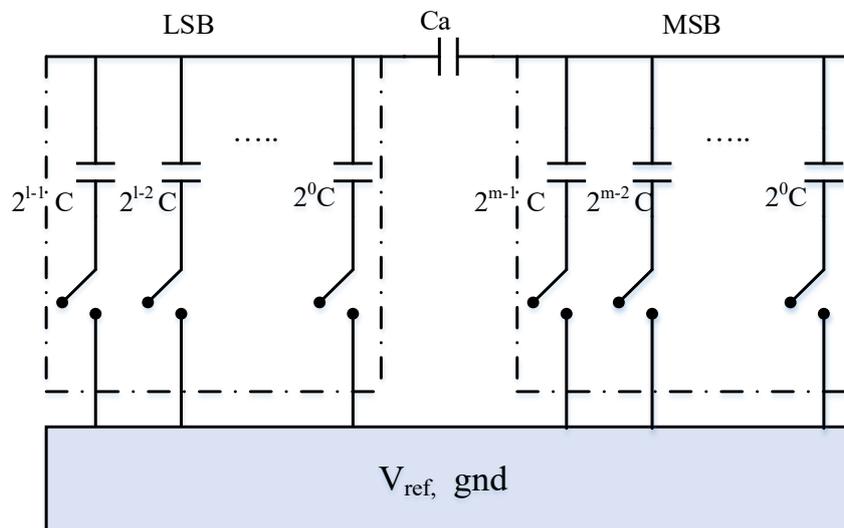


Figure 10: Design of two-stage subarray capacitor design

6. Delta Sigma ADC Design in Biomedical Sensor Application

The high-resolution, low-noise digitization of analog signals offered by delta-sigma ADCs makes them ideal for use in biological sensor applications. Their attributes render them very suitable for accurately capturing the minute and erratic signals commonly found in biological environments. Resolutions of 24 bits or more are attained by Delta-Sigma ADCs, which is essential for recording low-frequency changes in biosignals such as electrocardiograms, electroencephalograms, and electromyograms. In biomedical applications, where signals are frequently vulnerable to interference, delta-sigma ADCs' noise-shaping ability plays a crucial role in efficiently mitigating the influence of noise. The low power consumption of many delta-sigma ADCs is crucial for wearable or portable biomedical equipment. Due to their broad dynamic range and ability to accurately capture signals at both tiny and large amplitudes, these ADCs are suitable for a variety of biomedical sensor types. This section reviews the various delta sigma ADC designs for biomedical applications.

Chen et al. [39] created a fully differential amplifier (FDA) and sigma-delta modulator with the use of a cascade inverter for the application of ECG and EEG recording. Furthermore, the cascade structure successfully mitigates the effects of power supply, ground noise, and output distortion. The FDA increases the output swing and SNR. The modulator design is emphasized with bootstrapped switches, and finally, the digital code is ultimately generated. In order to prevent crosstalk generated by the switched-capacitor circuit in the DSM, two subthreshold band gaps supply amplifiers are intended. The quantization circuit is tailored to the modulator design in order to improve accuracy while maintaining high speed.

Yoon et al. [40] had designed dual integrating (DI) DSM in AFE for biomedical instrumentation. The AFE circuit had been adapted with a pre-amplifier and switched capacitor. DI-DSM employs two unique clock frequency types: one that is half the conventional frequency and the other that is the same as the conventional frequency. This provides enough time for crucial blocks to settle. In 2019, Somappa et al. [41] proposed a filter-based continuous time DSM (CTDSM) with a reduced area for biomedical application. The design had been implemented with the aid of inverters and resistors.

Hematti et al. [42] had continuous-time (CT) second-order DSM for biomedical applications in the year 2021. Here, the coefficients of DSM are optimized with a genetic algorithm. A dynamic Regenerative Latch was employed as a comparator in the quantizer since it is particularly efficient in terms of speed and power consumption. The chopping approach's primary purpose is to discriminate between noise and signal frequency ranges. The designed model attains a signal-to-noise distortion ratio (SNDR) of 94.28dB and an effective number of bits (ENOB) of 15.37 bits with a CMOS process of 180nm.

To improve overall performance, Hussain et al. [43] created a fourth-order delta-sigma modulator with a quantizer. Furthermore, the author modified the signal transfer function, and the model achieved an SNR of 143 dB. Yang et al. [44] created a delta-sigma ADC with an ENOB of 17.02 bits and an SNR of 104.2dB for ECG applications. To improve the gain of the ADC design, the switched capacitor was merged with the current-mirror push-pull operational transconductance amplifier and DC.

The delta modulation-based ADC was designed by Karimlou et al. [45] for wearable ECG sensors in 2022. The suggested ADC is built using TSMC's 0.18- μm at a maximum ENOB of 10.9 while consuming only 68.12 nW power from an external power source of 0.8 V. This ADC circuit uses around 0.02 mm^2 of silicon die space and delivers an SNDR of about 67.4 dB over the ECG signal bandwidth with a 4 kHz sampling frequency. Kavitha et al. [46] created a second-order Continuous-Time (CT) DSM at 180nm with a voltage of 1.8V. The cascade of Integrators Feed-Forward (CIFF) is adapted with the ADC design with ENOB of 17.06bits to reduce power consumption and design complexity.

For a power-efficient design with enhanced dynamic range, Liang et al. [47] designed third-order non-inverting continuous time SDM for ECG application. To enhance the efficiency of the design with improved gain, a programmable input gain coefficient and an embedded anti-aliasing filter are integrated, and they occupy an active area of 0.225 mm^2 . For biomedical

applications, Kavitha et al. [48] designed flexible AFE with a sigma-delta modulator by the integration of cascaded feed-forward topology. The design yields an ENOB and SNR of 17 bits and 106.7dB, respectively.

The above section deals with the survey of advanced delta sigma ADC design for biomedical sensor applications. The DI Delta-Sigma Modulator improves upon the original Delta-Sigma modulator architecture by employing a second integrator. This modification is critical in enhancing noise shaping, resolution, and overall performance. The dual integrator enhances the SNR and helps to further lessen the effects of high-frequency noise. More quantization noise suppression is possible due to the architecture's effective improvement in the noise shaping order. However, compared to a single integrator design, dual integration architecture is more complex. A larger chip area, greater design difficulties, and possibly higher manufacturing costs can result from this increased complexity. CT integrators function differently from discrete-time (DT) integrators. A cascade of two CT integrators is used in a second-order modulator. The modulator can withstand clock jitter more effectively due to its continuous-time operation, which makes it less susceptible to noise in biomedical applications. Compared to their discrete-time counterparts, CT modulators may be designed to function with less power, which makes them ideal for wearable and portable biomedical equipment that long need battery life.

Nonetheless, CT modulators may exhibit greater variability in performance across manufacturing runs due to their increased sensitivity to process variation during fabrication. Furthermore, non-idealities such as component mismatches and parasitic and non-linearities in the integrators and DACs are more noticeable to the CT modulators. If these non-idealities are not properly addressed, performance may suffer. An innovative design known as a fourth-order Delta-Sigma modulator achieves high-order noise shaping by sequentially using four integrators, which greatly improves noise performance and resolution. With each integrator, the signal is further smoothed, and the noise effect is gradually diminished. Superior noise shaping capabilities are offered by the fourth-order architecture, which raises quantization noise to extremely high frequencies. In particular, if the feedback loops are not properly designed, higher-order modulators are more vulnerable to stability problems. Careful tuning and frequently advanced control systems are needed to ensure stability.

7. SAR-ADC Design in Biomedical Sensor Application

SAR-ADC is frequently utilized in biomedical sensor applications because it balances speed, resolution, and power efficiency. SAR-ADCs are useful for capturing detailed biomedical signals like ECG, EEG, and other physiological data because they can reach high resolution, usually in the range of 12 to 16 bits. SAR-ADCs can process data at a rate that is sufficient for many biomedical applications yet inadequate for applications that need to convert data at a very high speed, such as high-frequency ultrasound imaging. They are ideal for wearable and portable medical equipment because of their great efficiency and very simple construction. To satisfy the unique needs of the intended application, their restricted dynamic range, noise

sensitivity, and speed restrictions should be taken into account during the design stage. This section reviews the various SAR-ADC designs for biomedical applications.

Tian et al. [49] proposed a multi-channel ECG capture filter design and ADC in the AFE. This research proposes a fourth-order current-cancellation subthreshold-source-follower low-pass filter (CS-LPF) that employs cross-coupling current cancellation technology to save chip area and power. Then, the ECG signals can be recorded and quantified using the AFE's SAR ADC. 50% capacitance reduction is accomplished by the completely differential low-pass filter, which uses only 4.8nW of power. The design of [49] is illustrated in Figure 11.

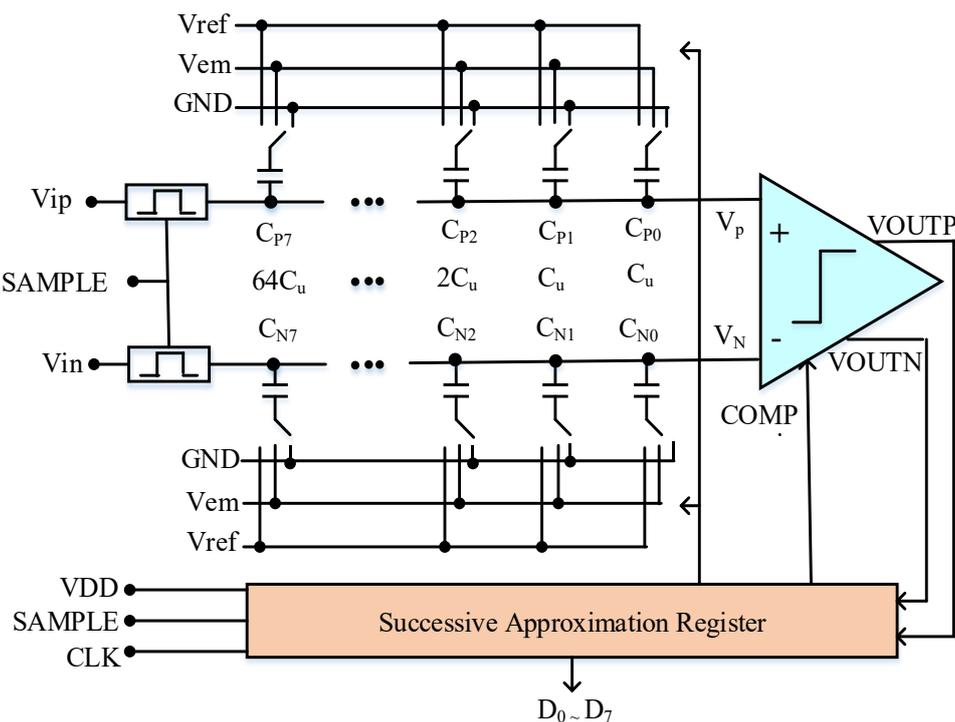


Figure 11: Schematic design of SAR-ADC [49]

Zheng et al. [50] designed a fully integrated AFE with a chopper amplifier (CA), DC servo loop, sampler, and SAR ADC. The sampler may reduce the aliasing effect and ripples. In this case, the capacitor ratio is decreased by using offset-compensated switched capacity, and the flicker noise is subsequently reduced by using CA. There are multiple stages to the introduction of the SAR ADC: bit cycling, auto zeroing, sampling, common-mode setting, and purging. In the ADC design, the latch comparator is utilized, and the AFE is operated under a power supply of 1.2V. For additional low-speed sensor applications, the ADC can be recycled. Lastly, the prototype chip was used by the authors to measure the human ECG, confirming the innovation in real-world applications.

Yang et al. [51] created a low-noise AFE design for long-term ECG monitoring in 2021. Pulse width modulation (PWM) was utilized to cancel the offset, and a dynamic scale ADC used a low-power comparator approach to produce a suitable dynamic margin to protect against signal loss. The regulated word registers, chopper amplifier, and dynamic scale sigma-delta

ADC are all components of the ultra-low power AFE, which has an SFDR of 71.6 dB. The recommended AFE achieves a NEF of 2.4 while consuming 4 W of power. The design of [51] is illustrated in Figure 12.

Wang et al. [52] created a SAR ADC with a 0.3V supply voltage for biological applications. Weight biasing calibration was utilized to rectify the offset voltage without slowing down the comparator's operation. A unity-gain buffer was implemented to limit the influence of parasitic capacitances on the ADC. The initially uneven balance can be brought to equilibrium using the weight adjustment strategy. In order to achieve equilibrium and account for the comparator's bias or offset, appropriate weights are assigned prior to the comparator commencing the comparison.

Using the variable threshold approach, Mandrumaka and Noorbasha [53] developed a 10-bit SAR ADC with increased gain for use in biomedical applications. The ADC is highlighted by numerous components, including sample and hold, comparator, and register. SAR control logic uses the comparator output to regulate the DAC switches. A simple sample and hold circuit is constructed using a CMOS transmission gate and a sampling capacitor. In the experimental scenario, several measures such as DNL- + 0.9/- 0.82 LSB and INL- + 0.9/- 0.82 LSB, ENOB- 7.69, and SFDR- 68.54dB are examined and compared with existing ADC designs.

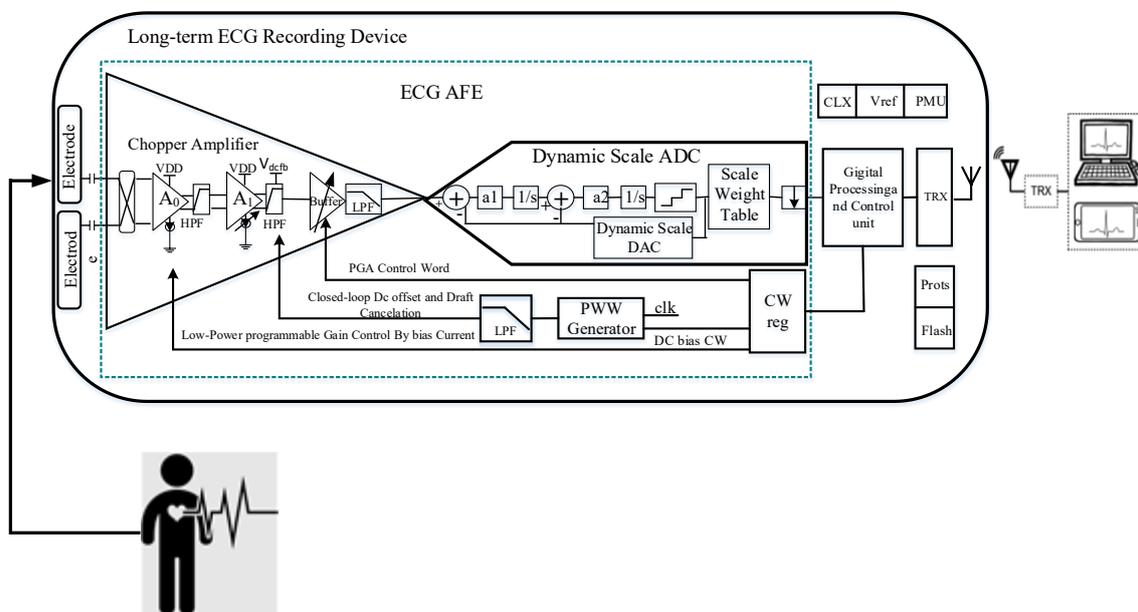


Figure 12: AFE design of ECG system [51]

High-speed power SAR ADC implemented by Naguib [54] for biomedical applications with dynamic latched comparator design. The pre-amplifier is located in the first stage of the comparator design, while the latch circuit is located in the succeeding stage. The design was created utilizing 180nm technology and a 1.2V supply voltage.

Vafaei et al. [55] created a SAR ADC using a 70% power-reduced new dynamic single trial structure-based comparator and power reduction approaches. The designed model had been verified in terms of ECG and EEG signals. Here, the designed model attains ENOB of 8.53 bits, SFDR of 62.47dB, SNDR of 53.13dB, differential non-linearity (DNL) of +0.46/ - 0.95, integral non-linearity (INL) of +2.54 /- 2.74, and power of 1.21nW respectively.

Karimlou et al. [56] designed a time-based ADC for ECG sensor application, and the model is designed in 180nm technology with a supply voltage of 0.8V. The complexity of the ADC converter is reduced, and it consumes 163 nW of power by generating 1-bit stream data. Mahmoud et al. [57] designed SAR-ADC for ECG detection systems by consuming 1.87 μ W under the supply voltage of 1V. The design was simulated in TSMC 0.25 μ m technology with ENOB of 6.5 bits, respectively. Thamaraimanalan and Sampath [58] created an ADC by modifying a variable resolution controller based on fuzzy logic. Furthermore, the power gating technique is used for power consumption in 90nm CMOS technology with a supply voltage of 1V and a frequency of 1MHz. The design was evaluated in terms of power and complexity during the simulation phase.

Singh and Tripathi et al. [59] developed a 16-bit SAR ADC with a comparator to save electricity. The amplitude of the applied bioelectric signals ranges between 10 V and 100 mV. The proposed SAR-ADC can be built with a sample rate of 500 MS/s using 45-nm CMOS technology and 0.45 mm² of area.

Zhang et al. [60] created a WBSN-specific code recombination-based ADC architecture. To cut down the bit cycle and power consumption, the search forward and backward procedures are integrated into the quantization stage. The ADC was designed, and it attains an SNDR and SFDR of 58.34 and 70.2 dB with 0.6V supply voltage. The ADC consumes only 40 nW of power and achieves a figure-of-merit (FoM) of 6.2 fJ/conversion step.

Ramkumar et al. [61] designed a quantizer-based SAR-ADC design by consuming less power. The non-uniform quantizer is built on the non-uniformity of the ECG signal and is implemented by modifying the SAR approach. The design was realized in a 65-nm TSMC process with 0.6V. In addition to this, the design attains a DNL/INL of 0.288/0.869 with 167 nW power consumption.

Polineni et al. [62] used 180 nm standard CMOS technology to create an integrated switching capacitor-based programmable hybrid ADC (SAR, DSM) for biomedical applications. The folded cascade OTA amplifier with bias circuit had been designed with a maximum gain of 83dB and 0.86–98 μ W power consumption.

By utilizing CADENCE Virtuoso 45 nm technology, the comparator had been designed by Tyagi et al. [63] for SAR ADC under the supply voltage of 1V. A low-power CTDSM design with an active resistor-capacitor (A-RC) circuit was designed for ECG application in the year 2022 by Kim et al. [64]. The A-RC can function as a first integrator, which helps to reduce power usage. The total power consumed was 2.16 W, with a peak SNR of 80.1 dB, an SNDR of 78.4 dB, and a bandwidth of 250 Hz.

Zhao et al. [65] developed a single-ended SAR-ADC switching system for harmonic distortion and dynamic offset for biosensor applications. The prototype has a 0.02 mm^2 active area, consumes power of 94 nW at 0.6-V supply, and the design was assembled using 65-nm CMOS technology. Wearable devices, such as smartwatches and bracelets, have grown in popularity in recent years and are now widely used. For biomedical applications, Rodrigues et al. [66] created an asynchronous SAR ADC with a switching mechanism. The model attains an SFDR and SNDR of 73.19 dB and 61.36 dB, respectively.

The above section deals with the survey of advanced SAR-ADC design for biomedical sensor applications. SAR-ADCs provide a good balance between power consumption, resolution, and speed, making them a great option for biomedical sensor applications. While analyzing the aforementioned survey, CS-LPF based SAR DAC was employed for ECG signal acquisition with low power and low noise, respectively. Here, the current cancellation, subthreshold operation, and source follower configuration are intended to cancel out the unnecessary current components and provide low output impedance. However, there could be some signal attenuation when operating in the subthreshold zone due to decreased transconductance. Some authors have defined AFE design with CA and SAR-ADC design for biomedical devices. Here, the CA modulates the input signal to a higher frequency before amplification and then demodulates it back to its original frequency in order to reduce low-frequency noise and offset. However, the integration of modules tends to increase sensitivity to process variation, limited flexibility, and complexity of debugging. In certain configurations, AFE employs PWM for offset cancellation and a dynamic scale ADC coupled with a low-power comparator for prolonged ECG monitoring to effectively improve signal integrity and power efficiency. In order to optimize the resolution and dynamic range for varying signal amplitudes, ADC adjusts its input range in response to the features of the signal.

However, the real-time range adjustments for the ADC could result in a slight delay, which might cause issues in high-speed or high-precision applications. A high-speed power-efficient SAR-ADC design with a dynamic latched comparator has also been designed to perform fast and accurate digital conversion while effectively controlling power consumption. However, high-speed ADCs can generate more heat due to rapid switching and high-frequency operation. Effective thermal management is necessary to preserve performance and dependability. Some authors have introduced quantizer based SAR-ADC, and the incorporation of quantizer and SAR ADC improves the design performance. The model achieves high resolution and accuracy with precise digital representation. However, in order to reduce quantization noise and high errors, resolution quantizers are required. Also, the design requires error correction modules to attain an accurate digital output. The switched capacitor circuits with SAR-ADC designs maintain stability in the accurate sampling and conversion process. Also, the model tends to optimize both speed and accuracy rapidly. Single-ended SAR differential designs are simpler than ADC designs, which can lower system costs and design complexity and also can achieve high speed conversion rates. However, the non-linearity in the switching system may cause harmonic distortion to affect the design. This distortion may have an impact on the digital representation of the analog signal's accuracy, especially in high fidelity applications.

8. AFE based Amplifier in Biomedical Sensor Application

A device that receives a signal as input and outputs an improved version of that signal is called an electronic amplifier. While designing an amplifier, several factors such as gain, bandwidth, figures of merit (FOM), linearity, noise, input offset voltage, input impedance, slew rate, efficiency, and stability are essential in accordance with the needs of the application. The research regarding amplifier designs is reviewed in this section.

The current mode AFE design was proposed for biomedical application by Krishnamoorthy et al. [67] in the year 2021. The design depicts a second current mode low-pass filter (CM-LPF) and a programmed gain current mode (PGCM) amplifier. In order to execute the switching action, the biasing is carried out in a way that causes the transistors to alternate between their cut-off area and saturation zone of operation.

AFE with inverter-based amplifiers was designed for biomedical application by Vafaei et al. [68] in the year 2021 by cascading the LNA and PGA simultaneously. Here, the author designed inverter-based LNA to attain an input impedance. An essential variable in biomedical amplifiers is the input impedance. Also, to enhance the gain of the amplifier, the gain boosting model was employed, and the chopper technique was utilized to eliminate the presence of noises. To cut down the power consumption, the author makes use of a common mode feedback circuit, and for biosignal acquisition, the PGA has been designed. In the experimental part, several measures, such as power, noise, gain, bandwidth, and area, are evaluated. The design of [68] is illustrated in Figure 13.

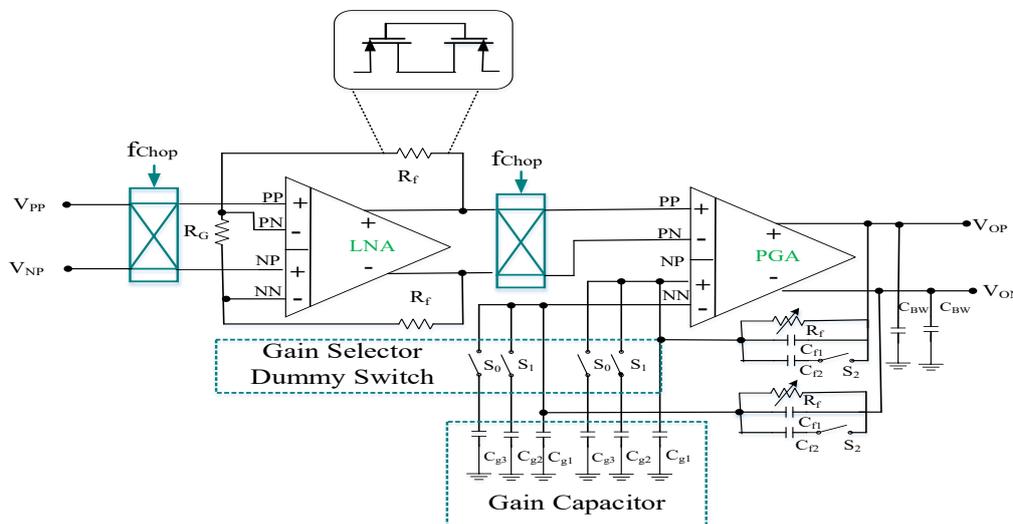


Figure 13: AFE design with LNA and PGA in [68]

Applications for biomedical technology are incredibly diverse, and LNAs play a major role in ECG and EEG systems. An LNA is a critical circuit. At supply voltages ranging from 1 to 1.8 V, LNAs have been modelled and implemented at 180, 90, and 65 nm. For various LNA designs, there is a 99.9% power variation, 103.7% bandwidth variation, 93.18% gain variation, 91.17% noise figure variation, and IIP3 97.5% area variation. A comparison of AFE

architectures revealed 93.54% highest performance, 79.78% maximum bandwidth, and 85.07% best power reductions [69].

Kosari et al. [70] designed an AFE for ECG and arrhythmia diagnosis with low-power circuit designs. The AFE was developed using a three-stage fully differential AC-coupled amplifier, which provides tunable gain and bandwidth for the acquisition of biosignals. A low-noise instrumentation amplifier (LNA), a tunable bandwidth low-pass filter (LPF), and a variable gain amplifier (VGA) make up the three stages of the AFE. The LNA utilizes capacitive feedback topology to attain a high common mode rejection ratio (CMRR) through several key mechanisms. Two input signals of different phases are normally delivered into the amplifier using a differential input configuration used by the LNA. As the differential amplifier amplifies the difference between the two inputs while rejecting signals that are the same on both inputs, this configuration naturally minimizes common-mode signals or noise that is common to both inputs. Capacitors are used to feed some of the output signal back to the input in a capacitive feedback system. This feedback loop enhances linearity, lowers distortion, and stabilizes the amplifier's functioning. In particular, capacitive feedback aids in preserving high input impedance, which reduces the loading effect and guarantees that the amplifier rejects common-mode inputs and remains sensitive to differential signals. Achieving a high CMRR can also be accomplished by ensuring that the resistors and capacitors in the differential paths are well matched. Any mismatch has the potential to cause imbalances that lower the CMRR. The feedback channels are symmetrical and ensure that the common-mode signals are reduced equally, and the capacitive feedback aids in preserving equilibrium. Common-Mode Feedback (CMFB) circuit senses the common-mode voltage at the output and corrects it to the appropriate level. This further enhances the rejection of common-mode signals by stabilizing the output common-mode level. The LNA with capacitive feedback architecture can efficiently suppress common-mode signals by combining these techniques, which results in a high CMRR. The design of three stage AFE is illustrated in Figure 14.

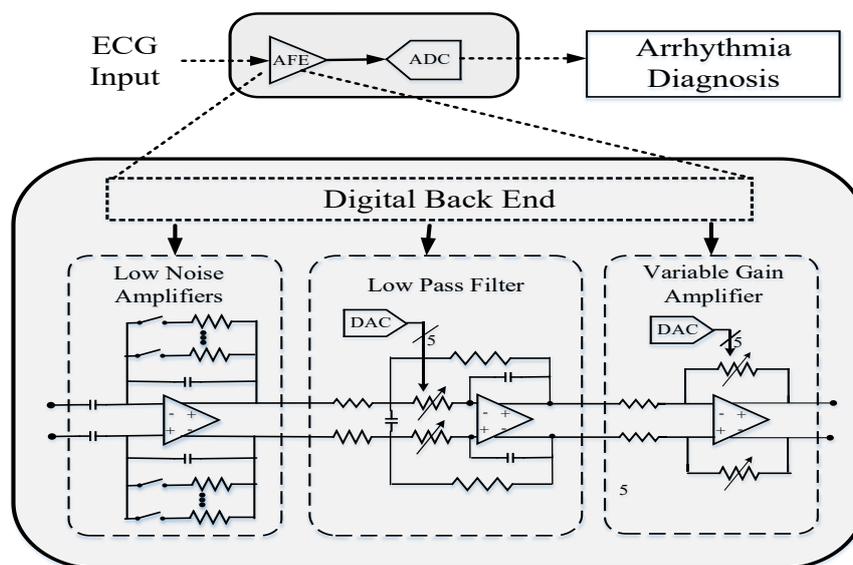


Figure 14: Design of AFE in [70]

Kumar et al. [71] designed a novel amplifier design AFE for ECG application in the year 2023. The AFE with DC coupling was designed by combining the instrumentation amplifier (IA) with PGA for low power consumption. In this study, researchers developed an AFE with DC coupling that combines an Instrumentation Amplifier (IA) with a PGA that has an AC-connected input stage. Under a voltage of 1.8V and a 0.18- μm CMOS implementation, the developed AFE offers a good gain of 76dB and a CMRR of 127dB, respectively.

The LNA and VGA had been designed for the ECG system by Panchal et al. [72], and these are the essential blocks of the AFE design. The two-phase operational transconductance amplifier (OTA) attained a gain of 45.9dB, and the VGA attained a gain of 25dB with a supply voltage of 1.8V. Yang [73] designed an AFE amplifier with the aid of a Driven-Right Leg circuit (DRL) under the supply voltage of 0.7V. Here, the two-stage inverter-based OTA amplifier is designed to attain a high CMRR. The power consumption and CMMR of the design is 4.32 μW and 132.2 dB, respectively. Yunfu [74] had an OTA ECG amplifier with increased gain and power efficiency in the year 2023. Here, initially, the ECG signal denoising process takes place to remove noise interference. The OTA was designed with 3.6V, and it overcomes the frequency distortion issues with better power consumption.

Nagulapalli et al. [75] proposed a VGA improvement technique in an AFE design for ECG application in 65 nm technology. The majority of existing VGA architectures have poor linearity because of low local feedback loop gain. Therefore, the additional feedback was insisted on in the current source terminal to enhance the loop gain of the design. In order to consume power of 0.43 μA , the design requires a 1.2V supply with an area utilization of 3,108 μm^2 respectively. The design of [75] is illustrated in Figure 15. Pritty and Jhamo [76] designed a current mirror-based OTA for ECG applications with enhanced bandwidth. The design had been operated under 0.8V with a CMRR of 145.47dB.

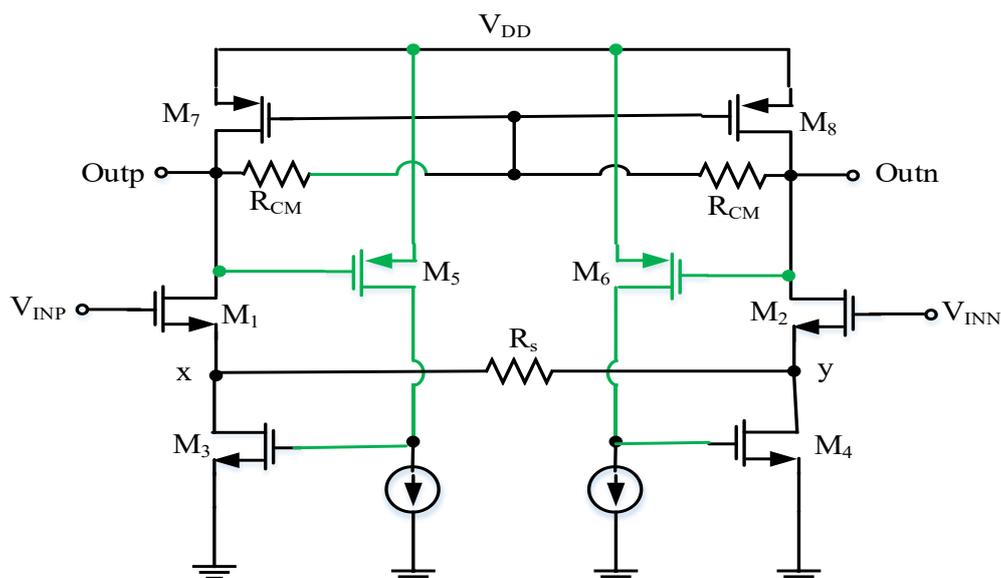


Figure 15: Design of VGA [75]

For ECG signal acquisition, Han et al. [77] designed PGA with a biasing technique, the capacitor-coupled instrumentation amplifier was also designed. The proposed design had been verified 0.13 μm CMOS technology under 1.2V and attained power of 0.6 μV . Also, the model yields a CMRR and PSRR of 93 dB and 77 dB consecutively. For signal acquisition of ECG/EEG application, Ahmad et al. [78] designed tunable feedback IA with dual bandwidth. The model reaches a CMRR of 143.19 dB under the supply voltage of 1.2V.

9. Justifications for ADCs and Amplifiers

A detailed parametric evaluation is given for SAR ADCs, AFE amplifiers, and Delta-Sigma ADCs in order to support the numerical comparison. In order to assist researchers in selecting the best design for certain biomedical applications, the tables 3 and 4 offer numerical insights into ADC and amplifier trade-offs.

Table 3: Comparison of Delta-Sigma and SAR ADCs in Biomedical Sensors

Parameter	Delta-Sigma ADC	SAR ADC
Power Consumption	Moderate (optimized for continuous monitoring)	Very low (best for wearable applications)
Resolution	High (16–24 bits)	Moderate (8–14 bits)
Speed	Low to moderate (suited for low-frequency biosignals)	High (suited for real-time processing)
Noise Performance	Superior (inherent noise shaping)	Requires post-filtering
Application Suitability	ECG, EEG, EMG (high-precision, low-bandwidth signals)	Wearable biosensors (low-power, fast conversion)

Table 4: AFE-Based Amplifier Performance Analysis

Parameter	Low-Noise Amplifier (LNA)	Programmable Gain Amplifier (PGA)	Variable Gain Amplifier (VGA)
CMRR (dB)	>90 dB (best for interference rejection)	70–80 dB (moderate)	60–75 dB (adjustable trade-off)
Input-Referred Noise	Very low (optimized for biosignal acquisition)	Low	Moderate
Power Consumption	Low	Moderate	Low to high (depending on gain control)

Application	High-precision biomedical signal acquisition	Adaptive gain control in ECG/EEG	Dynamic range extension
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10. Parametric Analysis of Biomedical AFE Design

The performance of the entire system is determined by a number of interdependent parameters that drive the design of a biomedical AFE. Through an evaluation of important trade-offs and their effects on biomedical signal acquisition circuits, this section offers a thorough parametric analysis. The analysis is based on measured and reported data across different AFE implementations.

10.1 Hierarchical Trade-off in AFE Design

Gain, bandwidth, noise, linearity, power consumption, and area efficiency are some of the performance parameters that are used in AFE design. The importance of the base vs the tip of the triangle varies according to the needs of the biological AFE application. Power efficiency is the primary design factor in low-power wearable ECG systems, frequently at the expense of low linearity and decreased bandwidth. On the other hand, low-noise performance is valued in high-precision EEG applications, which calls for design techniques that may result in higher power consumption. The base parameters of the triangle (e.g., noise, gain, and bandwidth) serve as foundational design constraints, while the tip parameters (e.g., power efficiency, linearity, and area) offer secondary optimization flexibility.

Key Insights from Triangle Representation:

- Low-noise AFEs prioritize gain-bandwidth performance but may require increased power consumption.
- Ultra-low-power AFEs optimize power and area constraints but often compromise linearity.
- High-linearity AFEs enhance signal integrity but demand higher power and increased circuit complexity.

10.2 Analysis of Key Parameters and Their Interdependencies

A comparative analysis of several AFE parameters is shown in Table 3, emphasizing the way that they affect circuit performance. This section offers a systematic examination of how various criteria impact one another and the overall system design.

10.2.1. Linearity (THD) vs. Power Consumption

The capacity of an AFE to maintain the quality of the input biomedical signal without introducing harmonic distortion is determined by linearity, which is frequently measured using Total Harmonic Distortion (THD). However, increasing linearity typically involves advanced

circuit techniques such as high-order feedback loops or digital linearization, both of which demand additional power.

Observations from Table 3

- Enhanced signal processing and linearization techniques result in higher power consumption ($> 50 \mu\text{W}$) for designs with lower THD ($< 0.1\%$).
- In contrast, AFEs designed for ultra-low-power ECG acquisition ($\sim 5 \mu\text{W}$) show higher THD values ($> 0.5\%$), indicating a trade-off between linearity and power efficiency.

Implication: Low-THD circuits are required for high-precision diagnostics at the expense of higher power consumption, whereas intermediate linearity may be acceptable for wearable and long-term monitoring applications in favour of longer battery life.

10.2.2. Gain vs. Noise Performance

The gain of an AFE directly affects input-referred noise performance, indicating its capacity to amplify weak biological signals. However, excessive gain can exacerbate thermal and flicker noise, leading to signal degradation.

Observations from Table 5

- Due to the amplification of circuit-induced noise components, AFEs with high gain ($> 60 \text{ dB}$) typically show higher noise levels ($> 2 \mu\text{V RMS}$).
- To balance noise control and amplification, designs optimized for low-noise applications (such as EEG recorders with $< 0.5 \mu\text{V RMS}$ noise) usually run at moderate gain levels (30–40 dB).

Implication: Gain and input-referred noise must be carefully balanced in low-noise biomedical sensors to guarantee the best possible signal quality without amplifying noise sources.

10.2.3. Bandwidth vs. Power Efficiency

An AFE's capacity to record rapid changes in the signal is determined by its bandwidth. However, larger bias currents and faster transistor operation are needed to achieve better bandwidth, which increases power dissipation.

Observations from Table 5

- High-bandwidth AFEs ($> 100 \text{ kHz}$) are not appropriate for long-term wearable applications due to their power consumption, which exceeds $100 \mu\text{W}$.
- Low-power AFEs ($< 10 \mu\text{W}$) typically feature bandwidths below 10 kHz , limiting their application to low-frequency biosignals like ECG and respiration monitoring.

Implication: High-bandwidth AFEs are better suited for clinical-grade monitoring systems, whereas maximizing power efficiency at the expense of limited bandwidth is acceptable for wearable and battery-powered biomedical sensors.

10.2.4. Area Efficiency vs. Integration Complexity

AFE circuits designed for implantable or miniaturized **devices** must minimize area while maintaining functionality. However, area reduction often requires advanced fabrication techniques and higher integration complexity, which can introduce parasitic effects affecting performance.

Observations from Table 5

- Designs with a high integration density (less than 1 mm²) are more vulnerable to parasitic capacitance, which affects bandwidth performance and noise.
- Greater thermal stability and less cross-talk can be attained by using larger AFEs with relaxed area limitations (> 2 mm²).

Implication: Advanced fabrication techniques and circuit layout optimization are necessary for extremely small, implantable applications in order to minimize performance deterioration brought on by parasitic effects.

10.3 Summary of Key Findings

Based on the parametric analysis, the following conclusions can be drawn:

1. **Power vs. Linearity Trade-off:** In most cases, achieving good linearity (low THD) requires more compensation circuits, which raises power consumption. Low THD designs are necessary for applications like EEG and EMG however portable ECG monitors can withstand larger THD for longer battery life.
2. **Gain vs. Noise Optimization:** High-gain AFEs increase the amplitude of signals, but they also make noise sources stronger. To maximize the clarity of biological signals, a balanced strategy is needed.
3. **Bandwidth vs. Power Consumption:** High-bandwidth architectures are less appropriate for ultra-low-power applications since they require more power. It is crucial to optimize bandwidth according to the frequency of biological signals.
4. **Miniaturization vs. Parasitic Effects:** For wearable and implantable AFEs, reducing the circuit area complicates integration and may result in performance trade-offs that call for careful manufacturing and designing techniques.

These findings provide a structured approach for designing application-specific AFEs by balancing key performance parameters based on intended use cases. The ideal AFE for biomedical applications must concurrently meet the requirements shown in Figure 16. The parameter analysis of ADC design is shown in Table 5.

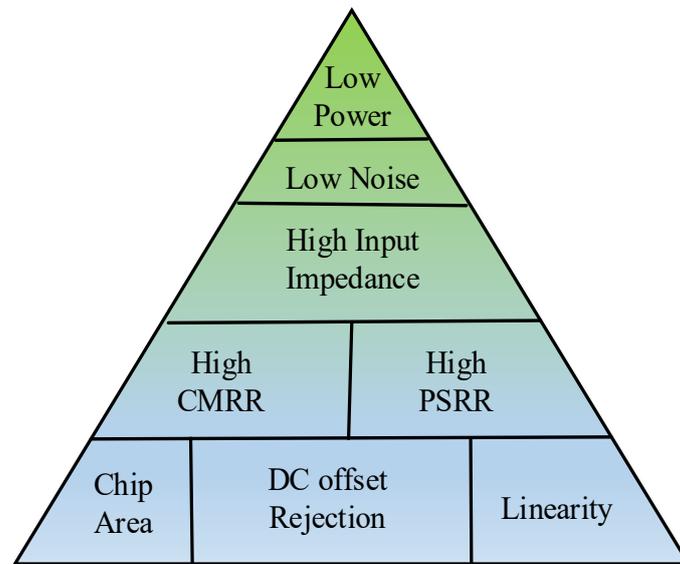


Figure 16: Parameter trade-off in a biomedical AFE

Table 5: Parameter analysis of ADC design

Reference	Parameters										
	Supply voltage (V)	SNDR (dB)	IRN (μV_r ms)	Bandwidth range	NEF	Area (m^2)	Power (μW)	Gain (dB)	THD	Process	Technology
68	0.8 V	N/A	1.4 μV	(0.9 – 100 Hz)	3.37	0.16 m^2	303 nW	71	24.6 dB	65 nm	CMOS
70	0.5V	N/A	2.8	155-250 Hz	2.78	0.24 m^2	68nW	52	N/A	130nm	CMOS
76	0.8V	N/A	6.33	N/A	N/A	N/A	29.52 μW	87.32	N/A	N/A	CMOS
78	0.18 V	N/A	0.58	0.1Hz-148.24 KHz	0.78	8194 μm^2	102.73 μW	67.9	N/A	0.18 μm	CMOS

39	0.6	66.7	3.976	10Hz-7KHz	2.67	1.68 m ²	8.4 μW	40	N/A	0.13 μm	CMOS
40	1 V	80.4	N/A	N/A	N/A	N/A	24.8 μW	N/A	N/A	65-nm	CMOS
49	N/A	N/A	2.68	0.3Hz-7KHz	1.81	0.96 m ²	4.8nW	56	N/A	65nm	CMOS
50	1.2V	63.2	2.38	0.64-6KHz	6.15	1.2 m ²	9.24 μW	58	0.082%	0.18-μm	CMOS
51	1.2V	71.6	3.27	N/A	2.4	0.53 m ²	4μ W	45.6	N/A	130nm	CMOS
52	0.3V	56.4	N/A	N/A	N/A	0.08 m ²	6.6 μW	75	N/A	90nm	CMOS
41	0.8V	38.8	N/A	N/A	1.57	0.068 m ²	0.37 μW	N/A	N/A	180nm	CMOS
53	0.5V	61.96	N/A	N/A	N/A	N/A	13.99 μW	N/A	N/A	180nm	CMOS
42	N/A	94.28	N/A	N/A	N/A	0.083 m ²	32.34 μW	N/A	N/A	180nm	CMOS
57	1V	57	N/A	N/A	N/A	N/A	1.87 μW	N/A	N/A	0.25 μm	CMOS
45	0.8V	67.4	N/A	N/A	N/A	0.02 m ²	68.12 nW	52	N/A	0.18-μm	CMOS

46	0.8V	954.5	N/A	N/A	N/A	N/A	24 μ W	N/A		180nm	CMOS
62	1.8V	N/A	N/A	N/A		0.28 m ²	0.86–98 μ W	N/A	<90dB	180nm	CMOS
47	1V	84.2	N/A	N/A	N/A	0.25 m ²	5.4 μ W	18dB.	N/A	65nm	CMOS
65	0.6-V	56.42	N/A	N/A	N/A	0.02 m ²	94 nW	N/A	N/A	65-nm	CMOS
66	0.5V	61.36	N/A	N/A	N/A	N/A	1.43 μ W	N/A	N/A	180-nm	CMOS

NEF- Noise efficiency factor, THD- Total harmonic distortion, SNDR-Signal to noise distortion ratio, IRN- Input referred noise N/A- Not available.

11. Discussion

SAR-ADCs are well known for their modest resolution and energy efficiency. According to findings in the literature, SAR-ADCs get an SNR of 65–75 dB, which is adequate for biomedical monitoring in real time while consuming limited power. Their asynchronous nature and small size make them ideal for biomedical equipment that runs on batteries. Recent developments in hybrid ADC designs have been investigated to maximize power efficiency and resolution by combining the benefits of SAR and Delta-Sigma architectures.

An examination of ADC architectures reveals that SAR-ADCs offer higher power efficiency and faster conversion rates, whereas Delta-Sigma ADCs are superior in noise suppression and resolution. According to studies, the performance of both ADC types is greatly improved when chopper-stabilized amplifiers and subthreshold biasing techniques are used in AFE circuits. Recent publications have also suggested digital backdrop correction and machine learning-based calibration methods to further increase ADC accuracy in biomedical applications.

Although many ADC designs for biomedical sensing have been investigated in previous studies, more work is required to maximize energy efficiency while preserving good resolution. An interesting direction for future research is the combination of sophisticated low-power circuit techniques, AI-assisted ADC calibration, and neuromorphic computing methodologies.

Furthermore, in order to evaluate the practicality of emerging hybrid ADC architectures, thorough experimental validation is required.

12. Challenges and Future Directions

Noise Reduction in Amplifiers: To capture weak bio signals without introducing an excessive amount of noise, LNAs are essential. A major problem, especially for wearable and portable biomedical devices, is obtaining ultra-low noise levels while preserving power efficiency. To further reduce noise levels without sacrificing power efficiency, research might focus on creating new materials, sophisticated circuit topologies, or noise-canceling methods.

Power Consumption: Ultra-low power consumption is necessary for biomedical sensors in order to prolong battery life, particularly for those utilized in wearable or implanted devices. A significant difficulty is achieving a balance between power efficiency and high-performance demands like low noise and high resolution. This problem might be solved with the aid of advancements in energy-harvesting methods, ultra-low-power circuit designs, and power management approaches. Furthermore, maximizing the trade-offs between noise, power, and resolution is still a crucial topic for further investigation.

High Input Impedance: In order to avoid loading effects on the signal source, amplifiers like VGAs and PGAs must maintain high input impedance. It's challenging to get high impedance without impacting other performance measures like stability and bandwidth. Future studies may examine innovative circuit architectures that boost input impedance while preserving or even enhancing bandwidth and stability. It might also be investigated to integrate sophisticated feedback mechanisms.

ADC Resolution and Speed: The high resolution of DSM and SAR based ADCs makes them popular in biological applications. However, it is difficult to maintain high resolution at fast speeds and minimal power consumption. Future advancements might concentrate on hybrid ADC designs that bring together the advantages of SAR and DSM architectures. Performance could also be improved by investigating novel quantization methods, oversampling schemes, and digital correction algorithms.

Miniaturization and Integration: The compilation of amplifiers, filters, and ADCs onto a single chip while maintaining performance is getting harder as biomedical devices get smaller. Crosstalk, parasitic capacitance, and thermal management problems are frequently brought on by miniaturization. Some of these issues may be addressed by the development of new materials and better production techniques like 3D integration. System-on-chip (SoC) systems that integrate the complete AFE while reducing power consumption and interference may also be the focus of intense research.

Interference and Crosstalk: Electromagnetic interference (EMI) is a common operating condition for biomedical sensors, and it can cause crosstalk and signal deterioration. Techniques for shielding and filtering are essential, but they can increase the design's complexity and size. It may be beneficial to conduct research into more sophisticated filtering methods and shielding materials that can be incorporated without expanding the sensor's overall size.

Future AFEs might have to accommodate multi-modal sensing, which processes several biosignals at once (such as electrical, chemical, and optical). The design of AFEs that can run on energy harvested from the human body (such as thermal or kinetic energy) may lessen or eliminate the requirement for batteries, resulting in longer-lasting and more environmentally friendly biomedical equipment.

13. Conclusion

This study has reviewed the most recent advancement in the ADC architecture design with multiple amplifiers in the AFE. ADC is a crucial design element since higher resolution and speed are needed at the same time. The performance of the entire system is significantly impacted by the ADC's design. There have been discussions on numerous implementation strategies for the main ADC components. This review study has described many circuit topologies, starting with the dynamic comparator, DAC, and S/H switching circuits. Multiple voltage switching techniques are also used to reduce the number of switches for ultralow power consumption. These methods can reduce the capacitance array's area while preserving switching energy and have excellent linearity. Additionally, ADC designs are used to speed up the conversion process. PGAs and VGAs have been extensively studied over the past 50 years, but they are being utilized more frequently. Also, new architectures and methodologies have just been proposed, which renders them a crucial research topic. Moreover, a viable path entails integrating ADC capabilities into other chips' microcontrollers, which would ultimately result in a decrease in the total system size and related expenses. Furthermore, new materials that go beyond silicon, like graphene, have the potential to make enormous advancements in ADC performance and capabilities. These materials hold great promise for the future of ADC development.

References

- [1] H. Dalmia, S.K. Sinha, Analog to digital converters (ADC) A literature review. In E3S Web of Conferences, 184 (2020) 01025. EDP Sciences.
- [2] S. Banu, S. Gupta, Low Power Analog to Digital Converter for Neuro Stimulator using Cadence Tool. In Journal of Physics Conference Series, 2325(1) (2022) 012005. IOP Publishing.
- [3] X. Nan, X. Wang, T. Kang, J. Zhang, L. Dong, J. Dong, P. Xia, D. Wei, Review of flexible wearable sensor devices for biomedical application. Micromachines 13(9) (2022) 1395.
- [4] G. Shen, Recent advances of flexible sensors for biomedical applications. Progress in Natural Science Materials International 31(6) (2021) 872-882.
- [5] C.H. Lin, K.A. Wen, An innovative successive approximation register analog-to-digital converter for a nine-axis sensing system. Journal of Low Power Electronics and Applications 11(1) (2021) 3.
- [6] H. Bhamra, J. Lynch, M. Ward, P. Irazoqui, A noise-power-area optimized biosensing front end for wireless body sensor nodes and medical implantable devices. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 25(10) (2017) 2917-2928.

- [7] M. Ortmanns, Wideband and low-power delta-sigma ADCs State of the art, trends and implementation examples. In ESSCIRC 2021-IEEE 47th European Solid State Circuits Conference (ESSCIRC), (2021) 28-35. IEEE.
- [8] M. Jotschke, W.C. Ossa, T. Reich, C. Mayr, A 10.5 μ W programmable SAR ADC front-end with SC pre-amplifier for low-power IoT sensor nodes. In 2020 IEEE 6th World Forum on Internet of Things (WF-IoT), (2020) 1-6. IEEE.
- [9] S.A. Zahrai, M. Onabajo, Review of analog-to-digital conversion characteristics and design considerations for the creation of power-efficient hybrid data converters. *Journal of Low Power Electronics and Applications* 8(2) (2018) 12.
- [10] S.L. Chen, J.F. Villaverde, H.Y. Lee, D.W.Y. Chung, T.L. Lin, C.H. Tseng, K.A. Lo, A power-efficient mixed-signal smart ADC design with adaptive resolution and variable sampling rate for low-power applications. *IEEE Sensors Journal* 17(11) (2017) 3461-3469.
- [11] M. Sadollahi, K. Hamashita, K. Sobue, C. G. Temes, An 11-bit 250-nW 10-kS/s SAR ADC with doubled input range for biomedical applications. *IEEE Transactions on Circuits and Systems I Regular Papers* 65(1) (2017) 61-73.
- [12] K. Park, D.J. Chang, S.T. Ryu, Brief overview on design techniques and architectures of SAR ADCs. *Journal of Semiconductor Engineering* 2(1) (2021) 99-108.
- [13] H. Ko, H. Kim, B. Lee, J. Kim, D.D. Cho, K. Han, Low-noise Analog Front-end with Chopper-stabilized Multipath Current-feedback Instrumentation Amplifier for Resistive Sensors. *Sens. Mater* 30 (2019) 1697-1706.
- [14] A. López, F. Ferrero, J.R. Villar, O. Postolache, High-performance analog front-end (AFE) for EOG systems. *Electronics* 9(6) (2020) 970.
- [15] M. Maslik, L.B. Leene, G. Timothy, Constandinou. *Analogue Front-End Design for Neural Recording. Handbook of Neuroengineering* (2020) 1-26.
- [16] M. Yoo, Y. Kwon, H. Kim, G. Choi, K. Nam, H. Ko, Low-noise resistive bridge sensor analog front-end using chopper-stabilized multipath current feedback instrumentation amplifier and automatic offset cancellation loop. *IEEE Access* 10 (2022) 12385-12394.
- [17] Z. Zhao, Y. Nai, Z. Yu, X. Xu, X. Cao, X. Gu, Design of Low-Power ECG Sampling and Compression Circuit. *Applied Sciences* 13(5) (2023) 3350.
- [18] W. Chen, Y. Zeng, Z. Li, J. Yang, Y. Li, A 41-nW SAR ADC with a FIA-based Comparator and a Bulk-driven Latch for ECG Applications. In 2022 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), (2022) 54-58. IEEE, 2022.
- [19] M.A. Serhani, H.T. El Kassabi, H. Ismail, A.N. Navaz, ECG monitoring systems Review, architecture, processes, and key challenges. *Sensors* 20(6) (2020) 1796.
- [20] I. Kim, Y. A. Bhagat, J. Homer, R. Lobo, Multi-modal analog front end for wearable biosensors. *IEEE Sensors Journal* 16(24) (2016) 8784-8791.

- [21] F. Wu, T. Wu, M.R. Yuce, An internet-of-things (IoT) network system for connected safety and health monitoring applications. *Sensors* 19(1) (2018) 21.
- [22] A. Affanni, Wireless sensors system for stress detection by means of ECG and EDA acquisition. *Sensors* 20(7) (2020) 2026.
- [23] E. Nemati, M.J. Deen, T. Mondal, A wireless wearable ECG sensor for long-term applications. *IEEE Communications Magazine* 50(1) (2012) 36-43.
- [24] V. Randazzo, J. Ferretti, E. Pasero, A wearable smart device to monitor multiple vital parameters—VITAL ECG. *Electronics* 9(2) (2020) 300.
- [25] H. Wu, J. Chen, X. Liu, W. Zou, J. Yang, M. Sawan, An Energy-Efficient Small-Area Configurable Analog Front-End Interface for Diverse Biosignals Recording. *IEEE Transactions on Biomedical Circuits and Systems* (2023).
- [26] P.T. Kalaivaani, R. Krishnamoorthi, Design and implementation of low power bio signal sensors for wireless body sensing network applications. *Microprocessors and Microsystems* 79 (2020) 103271.
- [27] K. Wen, Y. Shen, T. Wang, S. Liu, A low-noise high-precision analog front end system for biopotential signals recording application. *Analog Integrated Circuits and Signal Processing* 111(1) (2022) 103-115.
- [28] G.K. Soni, H. Singh, H. Arora, A. Soni, Ultra low power CMOS low pass filter for biomedical ECG/EEG application. In 2020 Fourth International Conference on Inventive Systems and Control (ICISC), (2020) 558-561. IEEE.
- [29] J. Liu, D.J. Allstot, Windowed Integration Sampling in Bio-Signal Front-End Design. In 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), (2020) 529-532. IEEE.
- [30] D. Thakur, K. Sharma, R. Sharma, Ultra low-power low-pass filter design for wearable biomedical applications. In 2021 Devices for Integrated Circuit (DevIC) (2021) 629-632. IEEE.
- [31] W. Bai, Z. Zhu, A 0.5-V 9.3-ENOB 68-nW 10-kS/s SAR ADC in 0.18- μ m CMOS for biomedical applications. *Microelectronics Journal* 59 (2017) 40-46.
- [32] H. Wang, A.K. Nagabhushana, S. Leitner, Exploiting uncertain timing information in time-based SAR ADCs. *IET Circuits, Devices & Systems* 14(3) (2020) 390-397.
- [33] S. Polineni, M. S. Bhat, S. Rekha, A switched capacitor-based SAR ADC employing a passive reference charge sharing and charge accumulation technique. *Circuits, Systems, and Signal Processing* 39(11) (2020) 5352-5370.
- [34] A.T. Ramkaj, M. Strackx, M.S.J. Steyaert, F. Tavernier, A 1.25-GS/s 7-b SAR ADC with 36.4-dB SNDR at 5 GHz using switch-bootstrapping, USPC DAC and triple-tail comparator in 28-nm CMOS. *IEEE Journal of Solid-State Circuits* 53(7) (2018) 1889-1901.

- [35] B.M. Kelly, A.T. DiLello, D.W. Graham, Reconfigurable analog pre-processing for efficient asynchronous analog-to-digital conversion. *Journal of Low Power Electronics and Applications* 9(3) (2019) 25.
- [36] S. Mahdavi, S. Kazeminiya, K. Hadidi, A 17 MS/s SAR ADC with energy-efficient switching strategy. *Analog Integrated Circuits and Signal Processing* 103 (2020) 223-236.
- [37] N.J. Dasarahalli, L. Tonse, M.S. Bhat, 11.39 fJ/conversion-step 780 kS/s 8 bit switched capacitor-based area and energy-efficient successive approximation register ADC in 90 nm complementary metal–oxide–semiconductor. *IET Circuits, Devices & Systems* 12(3) (2018) 249-255.
- [38] G.A. Fahmy, M. Zorkany, Design of a memristor-based digital to analog converter (DAC). *Electronics* 10(5) (2021) 622.
- [39] C. Chen, L. Chen, X. Wang, F. Zhang, A 0.6 V, 8.4 uW AFE circuit for biomedical signal recording. *Microelectronics journal* 75 (2018) 105-112.
- [40] Y. Yoon, Q. Duan, J. Yeo, J. Roh, J. Kim, D. Kim, A delta–sigma modulator for low-power analog front ends in biomedical instrumentation. *IEEE Transactions on Instrumentation and Measurement* 65(7) (2016) 1530-1539.
- [41] M.S.B. Somappa, A Compact Fully Passive Loop Filter-Based Continuous Time $\Delta\Sigma$ Modulator for Multi-Channel Biomedical Applications. *IEEE Transactions on Circuits and Systems I Regular Papers* 67(2) (2019) 590-599.
- [42] F. Hemmati, E.N. Aghdam, A low-power CT 2nd order Delta Sigma modulator using a new design methodology for biomedical applications. *AEU-International Journal of Electronics and Communications* 137 (2021) 153779.
- [43] A. Hussain, S. Ahmad, M. Ahmad, Z. Akbar, A 143 dB Delta-Sigma Modulator for Biomedical Applications. *International Journal of Emerging Multidisciplinaries Biomedical and Clinical Research* 1(1) (2023).
- [44] Y.T. Yang, H.J. Lai, L.H. Wang, M.H. Fan, A Delta-Sigma ADC Design for a Wearable ECG Application. In 2019 IEEE International Conference on Consumer Electronics-Taiwan (ICCE-TW), (2019) 1-2. IEEE.
- [45] A. Karimlou, M. Yavari, A Low-Power Delta-Modulation-Based ADC for Wearable Electrocardiogram Sensors. *IEEE Transactions on Circuits and Systems II Express Briefs* 69(9) (2022) 3670-3674.
- [46] M. Kavitha, S. Akhila, A. Kannan, Design and Implementation of a Second Order Continuous-Time $\Sigma\Delta$ Modulator for ECG Signal Acquisition. *Engineering, Technology & Applied Science Research* 13(1) (2023) 10128-10133.
- [47] J. Liang, S.W. Sin, U.S.Pan, F. Maloberti, R.P. Martins, H. Jiang, A high DR high-input-impedance programmable-gain ECG acquisition interface with non-inverting continuous time sigma-delta modulator. In 2019 IEEE Asian Solid-State Circuits Conference (A-SSCC), (2019) 309-312. IEEE.

- [48] M. Kavitha, S. Akhila, A. Kannan, Flexible Analog Front End Architecture for Biomedical Applications. In 2021 IEEE 3rd PhD Colloquium on Ethically Driven Innovation and Technology for Society (PhD EDITS), (2021) 1-2. IEEE.
- [49] Y. Tian, Z. Qin, Y. Yu, D. Gao, X. Liao, L. Liu, A Low-Noise and Low-Power Multi-Channel ECG AFE Based on Orthogonal Current-Reuse Amplifier. IEEE Transactions on Circuits and Systems I Regular Papers (2023).
- [50] J. Zheng, W.H. Ki, C.Y. Tsui, A fully integrated analog front end for biopotential signal sensing. IEEE Transactions on Circuits and Systems I Regular Papers 65(11) (2018) 3800-3809.
- [51] W. Yang, H. Jiang, Y. Yin, Z. Wang, A 4- μ W analog front end achieving 2.4 NEF for long-term ECG monitoring. IEEE Transactions on Biomedical Circuits and Systems 15(4) (2021) 655-665.
- [52] S.H. Wang, C.C. Hung, A 0.3 V 10b 3MS/s SAR ADC with comparator calibration and kickback noise reduction for biomedical applications. IEEE transactions on biomedical circuits and systems 14(3) (2020) 558-569.
- [53] K.K. Mandrumaka, F. Noorbasha, A low power 10 bit SAR ADC with variable threshold technique for biomedical applications. SN Applied Sciences 1 (2019) 1-9.
- [54] A. Naguib, High speed and low power comparator in 65 nm cmos for energy efficient biomedical sar adcs. In 2020 12th International Conference on Electrical Engineering (ICEENG), (2020) 339-342. IEEE.
- [55] M. Vafaei, M. R. Hosseini, E. Abiri, M. R. Salehi, A 0.2-V 1.2 nW 1-KS/s SAR ADC with a novel comparator structure for biomedical applications. Integration 88 (2023) 362-370.
- [56] A. Karimlou, M. Yavari, A time-based analogue-to-digital converter for ECG applications. In 2021 29th Iranian Conference on Electrical Engineering (ICEE), (2021) 154-158. IEEE.
- [57] S.A. Mahmoud, H.A. Salem, H.M. Albalooshi, An 8-bit, 10 KS/s, Successive Approximation Analog to Digital Converter in... CMOS Technology for ECG Detection Systems. Circuits, Systems, and Signal Processing 34(8) (2015) 2419.
- [58] T. Thamaraimanalan, P. Sampath, A low power fuzzy logic based variable resolution ADC for wireless ECG monitoring systems. Cognitive Systems Research 57 (2019) 236-245.
- [59] T. Singh, S.L. Tripathi, Design of a 16-bit 500-MS/s SAR-ADC for low-power application. In Electronic Devices, Circuits, and Systems for Biomedical Applications, (2021) 257-273. Academic Press.
- [60] Z. Zhang, Q. Yu, Q. Zhang, J. Li, K. Wu, N. Ning, A Code-Recombination Algorithm-Based ADC With Feature Extraction for WBSN Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 30(2) (2021) 134-142.
- [61] A. Ramkumar, A. Verma, B.P. Das, Ultra-Low Power Non-Uniform SAR ADC based ECG detector for Early Detection of Cardiovascular Diseases. In 2023 36th International

Conference on VLSI Design and 2023 22nd International Conference on Embedded Systems (VLSID), (2023) 92-97. IEEE.

- [62] S. Polineni, M.S. Bhat, A fully differential switched-capacitor integrator based programmable resolution hybrid ADC architecture for biomedical applications. *IET Circuits, Devices & Systems* 15(2) (2021) 141-155.
- [63] M. Tyagi, P. Mittal, P. Kumar, Simulation and Comparative Analysis of Dynamic Comparators at 1MHz for Biomedical Applications. In 2022 3rd International Conference on Issues and Challenges in Intelligent Computing Techniques (ICICT), (2022) 1-3. IEEE.
- [64] J. Kim, Q. Duan, J. Choi, C. Song, J. Roh, A 2.16- μ W Low-Power Continuous-Time Delta-Sigma Modulator With Improved-Linearity G_m for Wearable ECG Application. *IEEE Transactions on Circuits and Systems II Express Briefs* 69(11) (2022) 4223-4227.
- [65] X. Zhao, D. Li, X. Zhang, S. Liu, Z. Zhu, A 0.6-V 94-nW 10-Bit 200-kS/s Single-Ended SAR ADC for Implantable Biosensor Applications. *IEEE Sensors Journal* 22(18) (2022) 17904-17913.
- [66] M.C. Rodrigues, J.B.J. Brum, A.G. Girardi, L.C. Severo, P.C.C. de Aguirre, A 0.5-V 10-bit Asynchronous SAR ADC with Monotonic Switching for Biomedical Applications. In 2023 Argentine Conference on Electronics (CAE), (2023) 107-111. IEEE, 2023.
- [67] R. Krishnamoorthy, E. Kavitha, V. B. Geo, K. S. R. Radhika, C. Bharatiraja, A biasing based current mode analog front-end for biomedical applications. *Materials Today Proceedings* 45 (2021) 3113-3119.
- [68] A.L. Vafaei, E. Abiri, M. R. Salehi, A low power and ultra-high input impedance analog front end based on fully differential difference inverter-based amplifier for biomedical applications. *AEU-International Journal of Electronics and Communications* 142 (2021) 154005.
- [69] M.L. Pritty, Low-Power LNA in Analog Front End for Biomedical Applications. In *International Conference on Micro/Nanoelectronics Devices, Circuits and Systems*, pp. 299-324. Singapore Springer Nature Singapore, 2023.
- [70] A. Kosari, J. Breiholz, N. X. Liu, B.H. Calhoun, D.D. Wentzloff, A 0.5 V 68 nW ECG monitoring analog front-end for arrhythmia diagnosis. *Journal of Low Power Electronics and Applications* 8(3) (2018) 27.
- [71] A. Kumar, S. Balanethiram, DC-Coupled Fully Differential Difference Amplifier-Based Analog Front-End Design for Wearable ECG Sensors. In 2023 International Conference on Signal Processing, Computation, Electronics, Power and Telecommunication (IConSCEPT), (2023) 1-6. IEEE.
- [72] S. Panchal, S. Uniyal, S. Tantry, Design and implementation of low noise amplifier and variable gain amplifier for ECG systems. In 2022 IEEE 7th International conference for Convergence in Technology (I2CT), (2022) 1-6. IEEE.

- [73] Y. Yang, Design of Low-Power Low-noise CMOS ECG Amplifier for Smart Wearable Device. In Journal of Physics Conference Series, 1642(1) (2020) 012027. IOP Publishing.
- [74] Y. Ao, A Balanced OTA ECG Amplifier and Its Development Directions. Highlights in Science, Engineering and Technology 32 (2023) 150-156.
- [75] R. Nagulapalli, K. Hayatleh, S. Barker, A VGA Linearity Improvement Technique for ECG Analog Front-End in 65 nm CMOS. Journal of Circuits, Systems and Computers 29(07) (2020) 2050113.
- [76] M.J. Pritty, A 0.8-Volt 29.52- μ W Current Mirror-Based OTA Design for Biomedical Applications. Journal of Circuits, Systems and Computers (2023) 2350234.
- [77] W. Han, Q.Yu, K. Wu, Z. Zhang, J. Li, N. Ning, A programmable analog front-end with independent biasing technique for ECG signal acquisition. Microelectronics Journal 136 (2023) 105792.
- [78] R. Ahmad, N. Choudhary, S.K. Gupta, A.M. Joshi, D. Boolchandani, Novel tunable current feedback instrumentation amplifier based on BBFC OP-AMP for biomedical applications with low power and high CMRR. Integration 90 (2023) 214-223.
- [79] S. Ha et al., Integrated Circuits and Electrode Interfaces for Noninvasive Physiological Monitoring, IEEE Transactions on Biomedical Engineering, 61(5) (2014) 1522-1537 doi: 10.1109/TBME.2014.2308552.