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DESIGN AND IMPLEMENTATION OF ENERGY EFFICIENT ARITHMETIC AND LOGIC UNIT USING 45 NM TECHNOLOGY BASED ON HYBRID LOGIC ADDER

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Abstract:

The Arithmetic and Logic Unit (ALU) is a fundamental block of any digital processor, responsible for executing arithmetic and logical operations as its name suggests. In modern processors, ALUs are required to perform numerous mathematical operations rapidly on specific datasets. Therefore, improving operational speed while minimizing power usage directly enhances the overall throughput of the digital system. To achieve this, the ALU requires an adder circuit that offers high speed, low power consumption, and efficient performance.This work focuses on designing and implementing a compact, energy-efficient one-bit full adder by integrating Pass Transistor Logic (PTL) with the Transmission Gate technique. The adder design is optimized in terms of geometry to achieve better performance across power, area, and delay metrics. The proposed one-bit full adder cell exhibits desirable features such as low power dissipation and a reduced number of transistors. The architecture is implemented using 45 nm CMOS technology in the Micro Wind 3.9 environment. Furthermore, the proposed hybrid 1-bit adder design is scalable to a 16-bit ALU configuration while maintaining low power operation. The complete adder and ALU system function at a supply voltage of 1.2 V. Compared to conventional 17T and FA-11T designs, the proposed hybrid adder achieves approximately 30% reduction in power consumption.

Keywords: XNOR, XOR, Full Adder, Pass Transistor Logic, Transmission Gate, Hybrid logic, ALU.

I Introduction:

Recent portable electronics are defined by their functionality at low power supply levels and their design to support high switching frequencies. [1]-[2]. Numerous investigations have thus far documented the presence of various low-power and high-speed circuits. The complete adder functions as a fundamental component in various applications, including but not limited to Arithmetic Logic Units (ALUs), cryptographic systems, finite impulse response filters, and

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biochips. [3]-[8] As a result, numerous research have recorded various low-powered adder circuits. Numerous innovative concepts and techniques have been employed to construct entire adder circuits aimed at reducing power consumption, minimizing delay, and decreasing power-delay products, which have consistently been a primary area of research focus throughout the years.

The design styles are typically categorized into two types: 1) Static style and 2) Dynamic style.

In general, static full adders are known for their reliability, simplicity, and lower power consumption compared to their dynamic counterparts. However, they typically require more on-chip space than dynamic full adders. There are various logic design styles, each emphasizing different performance aspects. These include standard CMOS logic, Dynamic CMOS logic, Complementary Pass-Transistor Logic (CPL), Transmission Gate Adder (TGA) logic, and Pseudo-NMOS logic [9]-[10]. Among traditional logic types, Domino logic and Dual-Rail Domino logic are regarded as some of the most prominent. Many modern full adder designs employ a hybrid logic approach, combining multiple logic styles to optimize performance [11]-15]. By leveraging the strengths of different techniques, these hybrid designs aim to improve the overall efficiency, speed, and power usage of the full adder circuitry.

Traditional CMOS logic utilizes 28 transistors, offering the advantage of complete voltage swing operation. However, Complementary Pass-Transistor Logic (CPL), which employs 32 transistors [5]–[6], provides better voltage swing restoration but is less suitable for low-power applications. To overcome these drawbacks, a Transmission Gate (TG)-based adder architecture was developed, requiring only 20 transistors to realize full adder functionality. Pass Transistor Logic (PTL) has emerged as a more area-efficient approach for implementing full adders, as it substantially minimizes layout area [16]– [18].In recent years, there has been an increasing focus on hybrid circuit techniques [19]–[24], which combine multiple logic styles within specific modules to exploit the strengths of each. Although hybrid architectures deliver improved performance, they can face challenges such as reduced driving strength in cascaded stages unless appropriately buffered.

The main goal of this study is to enhance critical performance parameters—namely power consumption, propagation delay, and transistor count—when compared with conventional full adder designs. The proposed circuits are analyzed using 180-nm, 90-nm, and 45-nm CMOS technologies. Many contemporary full adder designs now adopt a hybrid logic methodology to achieve higher efficiency, faster operation, and lower power usage by integrating the advantages of various logic families.Section 2 covers the proposed XOR and XNOR. Section 3 outlines the proposed adder architecture and the design of the 8-bit ALU including the proposed adder. Section 4 discusses the findings of the simulations, including power analysis and layouts, while Section 5 ends the discussion.

II. Proposed XNOR and XOR circuits:

The presented circuit is a three-transistor XNOR gate implemented using CMOS technology. It comprises one PMOS and two NMOS transistors, each designed with distinct width-to-length (W/L) ratios.21]-[22]. The PMOS transistor (W = 0.8 μm, L = 0.045 μm) is connected to the

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supply voltage (VDD), while the two NMOS transistors (W = 1.2 µm, L = 0.045 µm and W = 1 µm, L = 0.045 µm) are connected to ground. This circuit takes two inputs, a and b, producing an output (out1) that follows XNOR logic—outputting a HIGH (1) when both inputs are equal (00 or 11) and a LOW (0) when the inputs differ (01 or 10).

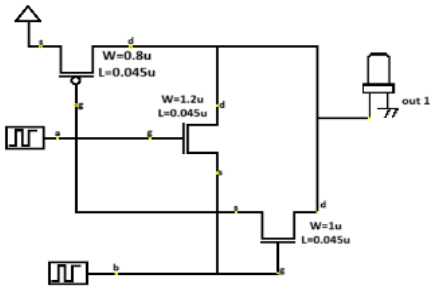
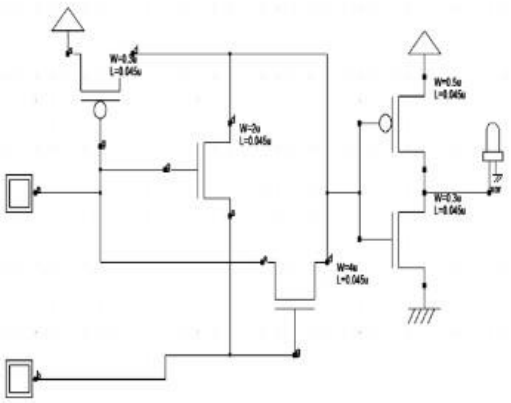


Figure1: Proposed XNOR gate

As shown in Figure 1, when both a and b are 0, the PMOS transistor turns ON, allowing current to flow and generating a HIGH output, while both NMOS transistors remain OFF. If one input is 0 and the other is 1, one of the NMOS transistors turns ON, pulling the output LOW. Conversely, when both A and B are 1, the PMOS transistor is activated again, resulting in a HIGH output. This streamlined design enables efficient XNOR operation using only three transistors [9]. From the proposed XNOR, it clearly shows that this efficient design reduces transistor count compared to conventional CMOS XNOR implementations, making it suitable for low- power digital logic circuits.

The proposed XOR circuit is illustrated in Figure 2.It takes two inputs, a and b, and generates a logic HIGH (1) when the inputs are different and LOW (0) when they are the same. The circuit operates through the complementary switching of the transistors. When A = B (00 or 11) the output is Low else A ≠ B (01 or 10) the output is High.

Figure 2: Proposed XOR gate



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This compact design achieves XOR functionality with minimal transistor count and efficient switching behaviour.

III. Design Methodology for the Proposed Full Adder

The circuit employs XOR/XNOR gates and multiplexers to create a full adder. A block creates XOR and XNOR output from inputs A and B, which are connected to a multiplexer controlled by the carry-in input C to get the Sum output Eq. (1) is the mathematical equation obtained from the 1-bit full adder in question, which computes the sum.

Sum = (C.(A XNORB)) +($\bar{C}$.(A XORB))... 1

sum = A XOR B XOR C.

The hybrid adder architecture generates the sum output by sequentially connecting hybrid XOR/XNOR elements with multiplexer components.

The carry generation of a designed adder, which is expressed by Equation 2.

$Carry = ((C.(A \oplus B)) + (B.(A \odot B)))$ 2

$carry = c(A\bar{B} + \bar{A}B) + B(\bar{A}\bar{B}+AB)$

$carry = AB + BC + CA.$

The hybrid logic style combines Pass Transistor Logic (PTL) with Transmission Gate (TG) logic to leverage the advantages of both methods, creating efficient, low-power digital circuits. PTL utilizes a reduced number of transistors by enabling inputs to directly manage signal pathways, which is advantageous for the implementation of components such as XOR/XNOR gates and multiplexers within the sum generation path. TG logic enhances PTL due to its susceptibility to threshold voltage loss, particularly when transmitting logic '1'. This approach utilizes both NMOS and PMOS transistors to ensure full logic swings and improved signal integrity. TGs demonstrate high efficacy in critical paths such as carry generation, providing precise and robust output levels. The hybrid approach, achieved through the combination of these two logic styles, results in reduced power consumption, minimized area, and improved performance in circuits such as one-bit full adders.

The proposed one-bit full adder functions based on the state of the carry-in (Cin), determining its operation according on whether Cin is 0 or 1. The total output is produced by a pass transistor logic (PTL) multiplexer [6]-[8], which utilizes XOR and XNOR outputs as inputs, employing Cin and its complement (Cin, derived from an inverter) as selection signals. This configuration allows the MUX to dynamically select the correct sum output based on the value of Cin—opting for the XOR output when Cin is 0 and the XNOR output when Cin is 1. A Transmission Gate (TG) based multiplexer is utilized for carry generation, selecting inputs based on the carry logic expressed as: Carry = C·XOR + B·XNOR. In PTL-based architecture, carry propagation is essential, and the OR operation with Cin enables efficient propagation while fulfilling the required logic. The carry output is delineated by Equation 2 in this configuration. The whole adder circuit utilizes XOR/XNOR gates and multiplexers, processing inputs A and B to produce both XOR and XNOR signals. The inputs are directed into a multiplexer (MUX) governed by

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Cin, facilitating the calculation of the sum as the aggregation of A, B, and Cin.

The proposed full adder is implemented using an XNOR/XOR -based circuit, requiring a total of 13 transistors is shown in figure3. The sum and carry-out (Cout) is derived using a combination of transmission gates and pass transistors, effectively implementing the required logic equations.

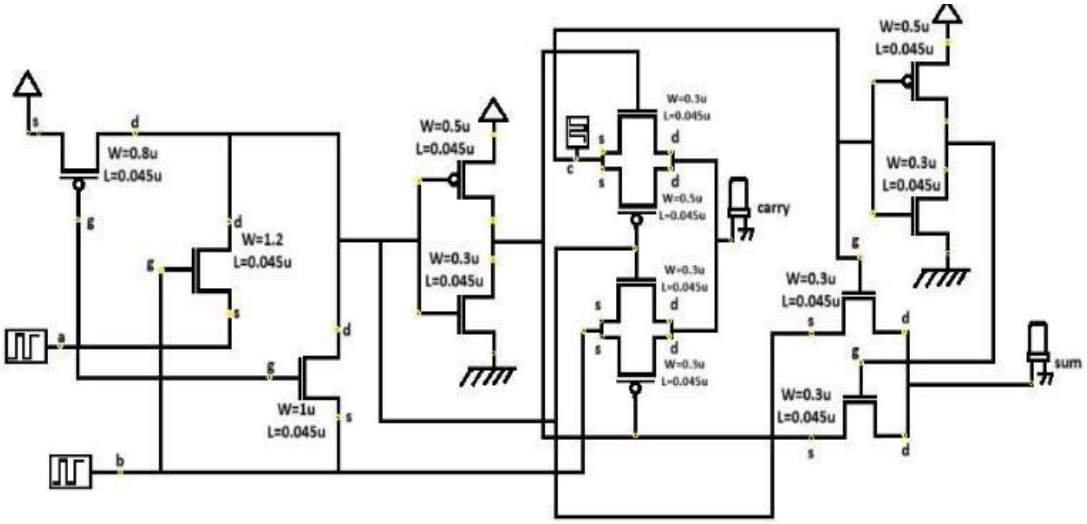

Figure 3: Proposed 1-bit full adder with 13- Transistor using hybrid logic

This adder design offers reduced power dissipation, fast operation for generating Sum and Carry signals, and resilience to device scaling.IV Proposed Design of ALU

Initially, the proposed 1-bit ALU cell is developed utilizing the proposed XOR gate, XNOR gate, and a 13T Full Adder. The ALU [35]-[37] performs arithmetic and logical operations using a combination of a full adder, multiplexers, and logic gates. For arithmetic operations, addition is carried out directly with the full adder, while subtraction is handled using two's complement by inverting one of the inputs and adding 1. The Functional table of proposed one bit ALU is shown in Table 1. There are two control signals: AS and AL. The AS signal indicates whether the operation is addition or subtraction—AS = 0 indicates addition, and AS = 1 indicates subtraction. The AL signal determines whether the ALU should execute an arithmetic or a logical operation. The proposed one bit ALU is shown in below figure 4.

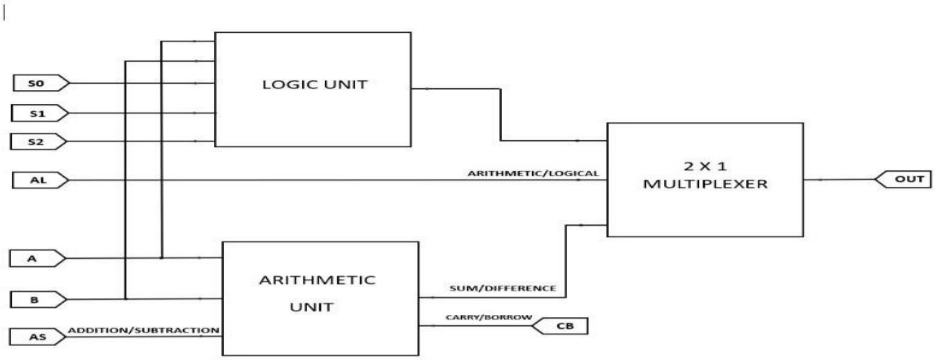

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Figure 4: Block Diagram of 1-bit ALU

The diagram above illustrates clear ALU architecture capable of performing both Arithmetic and Logical operations. It employs separate Arithmetic and logic units, which are governed by the input signals. The logic unit executes operations such as NOT, NOR, NAND, XOR, and XNOR based on the control inputs (S0, S1, S2), while the arithmetic unit handles addition or subtraction operations based on the AS signal. The final output from either the logic or arithmetic unit is selected by a 2x1 multiplexer, controlled by the AL signal during its operation. To enable easy inspection, LEDs indicate the result of the operation along with the carry/borrow status. The several operations that will perform by the ALU is shown in Table 1and Table 2.

Table1: Functional Table of 1-bit ALU

Modesignal	Opcode	
	0	1
AS	Addition	Subtraction
AL	Arithmetic Operations	Logical Operations

The ALU is designed for 6 different logical operations based on selection lines. the functional table of the proposed ALU logical operations is shown in table 2

Table2: Functional Table of one bit ALU

S0	S1	S2	OPERATION
0	0	0	No operation.
0	0	1	No operation.
0	1	0	~A
0	1	1	~B
1	0	0	NOR
1	0	1	NAND
1	1	0	XOR
1	1	1	XNOR

Multiple 1-bit ALUs are cascaded together to construct an 8-bit ALU. Each ALU processes a single bit of an 8- bit input to produce the final output. Proper propagation of carry in arithmetic operations is facilitated by the connection between the carry-out of one ALU stage and the carry-in of the subsequent ALU stage. The mode control signals shared by all ALUs are

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identical, ensuring that they perform the same operation across all bits. Overflow conditions in addition and subtraction can be identified with the help of the final carry-out from the last ALU stage. Symbolically, an 8-bit ALU is represented as a set of eight 1-bit ALU blocks connected in sequence, forming a complete unit capable of executing 8-bit operations efficiently. This modular approach simplifies the design and enhances the capabilities of a basic one-bit ALU to perform computations with multiple bits. The scalability of 1 bit ALU to 8-bit ALU is illustrated in figure 6 below.

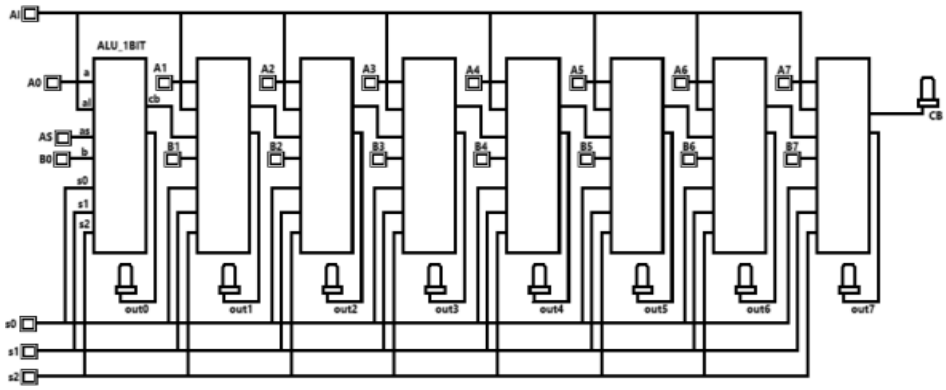

Figure 5: Proposed 8-bit ALU

IV. Results

Simulation Waveforms

The XNOR and XOR circuits being analysed were simulated using the Micro wind EDA tool version 3.9. The simulations were carried out utilizing 45nm process technology at a stable temperature of 27°C to maintain consistency across the comparative analysis. The simulation waveforms of XNOR and XOR circuits is shown in figure 6.

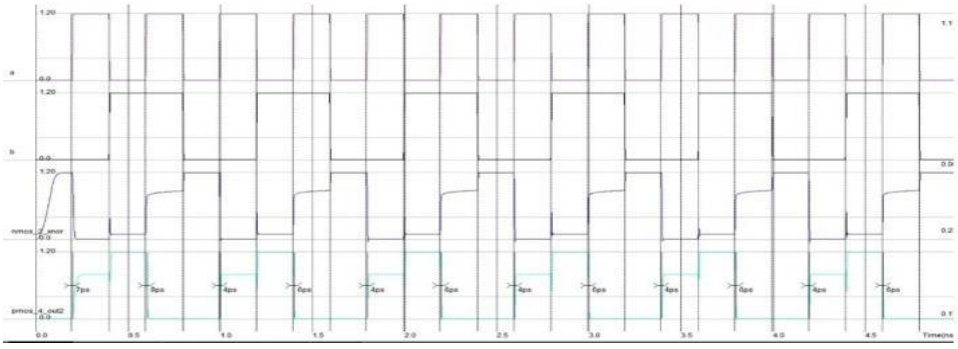

Figure 6: simulation Waveform of XNOR/XOR circuits

The simulation waveform of proposed 13 transistors one bit full adder is shown in Figure7.

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Figure 7: simulation Waveform of proposed one bit Full Adder circuit

A Full Adder accepts three inputs—A, B, and Cin—and produces a sum and a carry-out (Cout). When all inputs are zero, both the Sum and Cout are zero. If only one input is 1, the sum equals 1 and the carry-out remains 0. When both inputs are 1, the Sum equals 0 and Cout equals 1. Ultimately, when all three inputs equal 1, the Sum is 1 and Cout is likewise 1.

The logical operations performed by the ALU based on three control signals: S0, S1, and S2. When both S0 and S1 are 0, regardless of S2's value, the ALU performs no operation. When S0 is 0 and S1 is 1, the operation depends on S2: if S2 is 0, the ALU outputs the bitwise NOT of input A (~A); if S2 is 1, it outputs the bitwise NOT of input B (~B). The simulation waveform of 1-bit ALU is shown in Figure8.

Figure 8: simulation Waveform of proposed 1-bit ALU

When S0 is 1 and S1 is 0, the ALU performs NOR if S2 is 0 and NAND if S2 is 1. Lastly, when both S0 and S1 are 1, the ALU performs XOR when S2 is 0 and XNOR when S2 is 1.

b. Power Analysis (i)Full adder

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Table III shows the simulation results that compare the performance metrics of different full-adders, specifically focusing on power consumption, propagation delay, and Power-Delay Product (PDP). All full-adders underwent testing at supply voltages of 0.8 V and 1.2 V, with input signals functioning at a maximum frequency of 500 MHz. The results presented pertain exclusively to the full-adder circuit (add) in isolation. In certain instances, the power drawn from the power supply may be less than the total average power consumption. This discrepancy is observed in specific logic styles, including pass-transistor logic, where a portion of the current is derived from the input signals to charge the internal nodes of the circuit.

.Table 3. Comparison of proposed 1-bit full adder w.r.t previous adder designs.

Ref	**No of**	**Transistors**	**Average Power(µW)**

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Power Delay Product (PDP)

		0.8V	1.2V	0.8V	1.2V	0.8V	1.2V
25	32	84.8	37.3	1.72	3.89	145.9	145.1

Delay(ns)

26	28	125.8	39.7	0.68	1.91	85.5	75.8
27	24	128.4	65.9	0.76	1.68	97.6	110.7
28	24	189.1	60.2	0.78	2.31	145.6	139
29	23	81.4	35.1	0.54	1.35	43.9	47.4
30	22	77.3	28.6	0.63	1,49	48.7	42.6
31	21	90.53	39.7	0.61	1.32	55.2	52.4
32	20	132.3	50.4	0.7	1.79	104.5	90.2
30	18	98.8	31.8	0.46	1.09	43.5	34.7
33	17	85.6	42.4	0.78	1.17	66.76	49.6
34	16	145.6	66.8	0.61	1.33	88.8	88.8
33	16	81.6	38.7	0.44	0.98	35.9	37.9
proposed	13	69.5	29.4	0.37	0.81	25.71	23.81

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Figure 9 illustrates the comparative average power consumption between the previous full adder design and the proposed full adder.

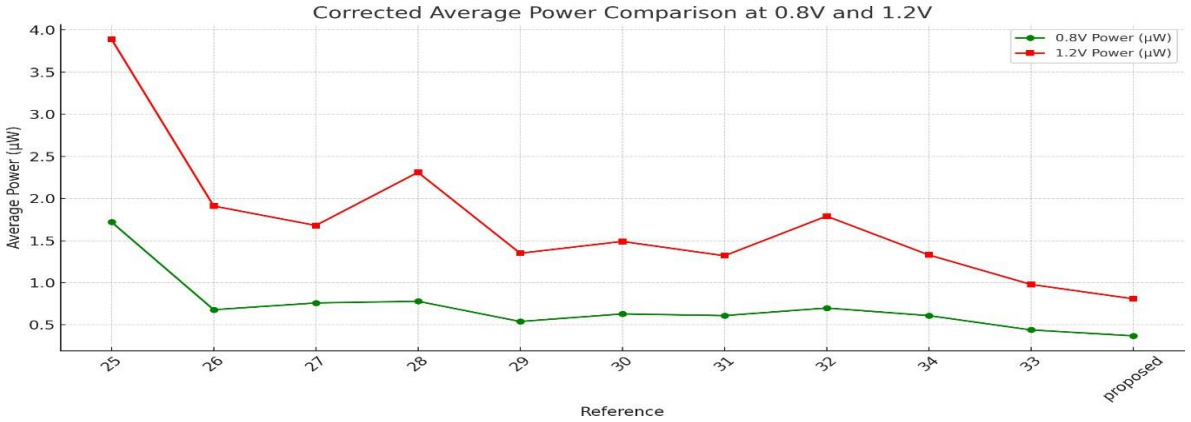

Figure9: power analysis of different adders at 0.8V and 1.2V supply voltage.

The average power usage has decreased by 15% at a supply voltage of 0.8 V and by 18% at an operating voltage of 1.2 V.

Figure 10 depicts the comparative delay analysis between the prior full adder design and the proposed full adder across various supply voltages.

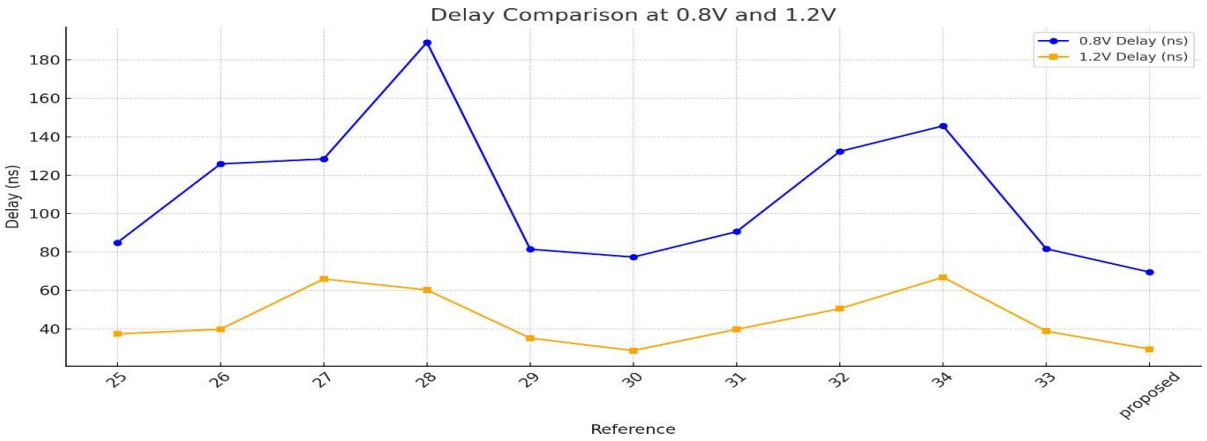

Figure10: Delay analysis of different adders at 0.8V and 1.2V supply voltage

The delay associated with the proposed 1-bit full adder has been substantially reduced in comparing with prior investigations. The proposed adder offers advantages in reducing power and delay.

Figure 11 displays the transistor count comparison with current methods.When compared to earlier methods, the graph clearly illustrates the suggested work constructed 1 bit full adder using 13 transistors.

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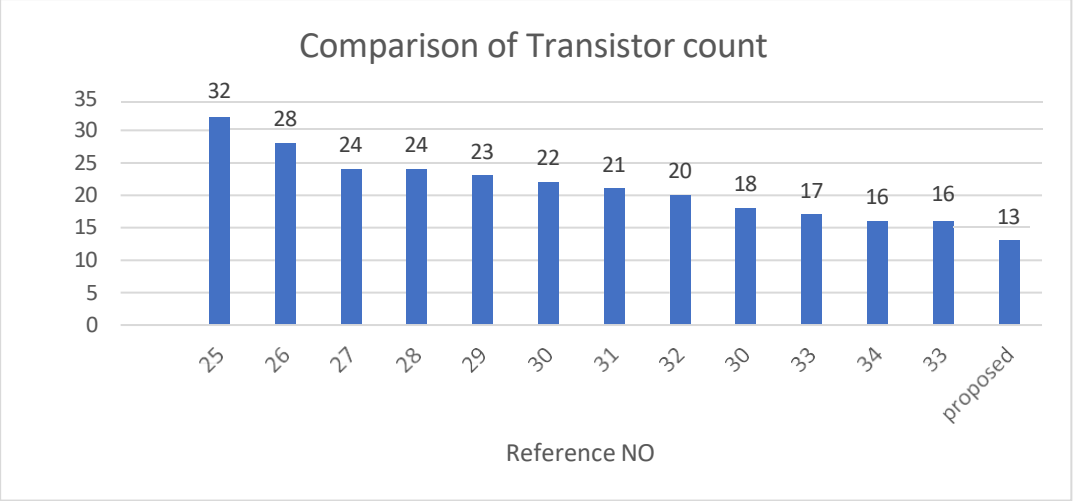

Figure11: Comparison of Transistor count

(ii) ALU

The simulation was carried out using the Micro wind EDA tool, version 3.9. The simulations were performed using 45nm process technology. The simulation results comparing the performance of various ALUs in terms of power consumption are presented in Table IV.

Table IV. Power Results (Power e-6w) for different data width of ALU

	Power(e-6W)	
Design	1-bit ALU	8- bit ALU
Ref no 35(Adder with 17T)	4.47	32.9
* With Proposed adder(13T)	3.82	26.30

The power consumption of a 1-bit ALU is lowered by 18%, while the 8-bit ALU shows a reduction of 20% when compared to the ALU design utilizing 17 transistors (17T) and the ALU design employing the proposed 13- transistor full adder (13T).

C.Layouts:

Layout denotes the physical manifestation of an integrated circuit, where in the abstract circuit design is converted into geometric patterns over several layers, including diffusion, polysilicon, metal, and vias. These layers define the fundamental components like as transistors and interconnects on silicon. The layout process must adhere to the design regulations established by the fabrication foundry to guarantee manufacturability, verified through Design Rule Check (DRC). Subsequent to layout, Layout vs Schematic (LVS) verification determines the symmetry of the layout with the original circuit, succeeded by parasitic extraction and post-layout simulation. The layout of proposed XNOR circuit is shown in figure 12.

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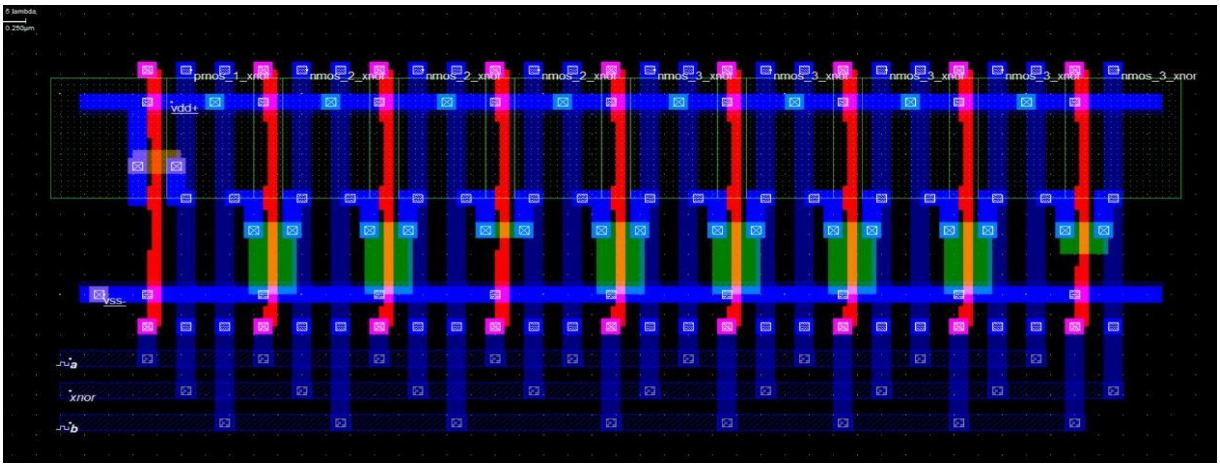

Figure 12: Layout of proposed XNOR circuit

Figures 13 and 14 depict the layouts of the suggested 1-bit Full adder with 13 Transistors and 8-bit ALU, respectively.

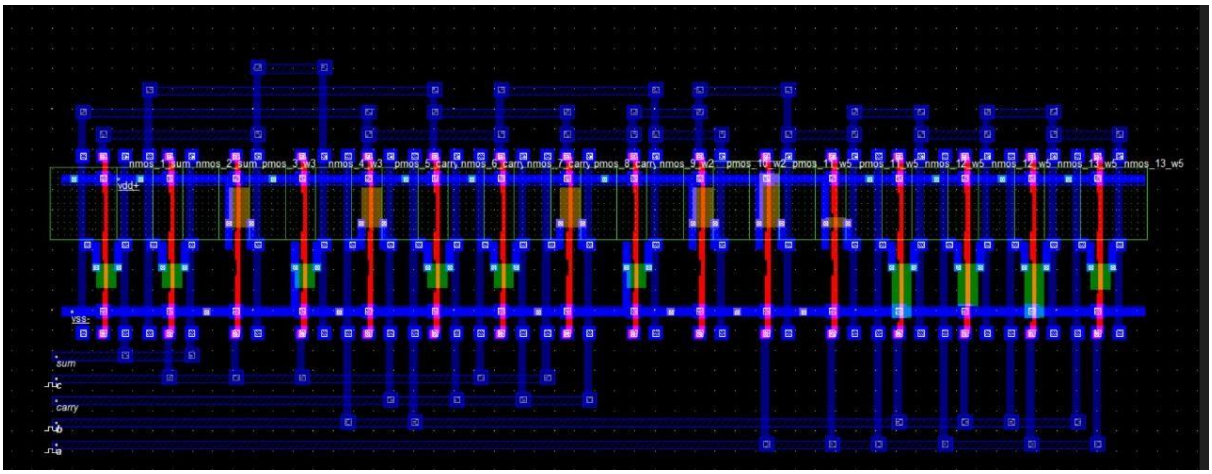

Figure 13: Layout of proposed 13 Transistor1- bit Full adder

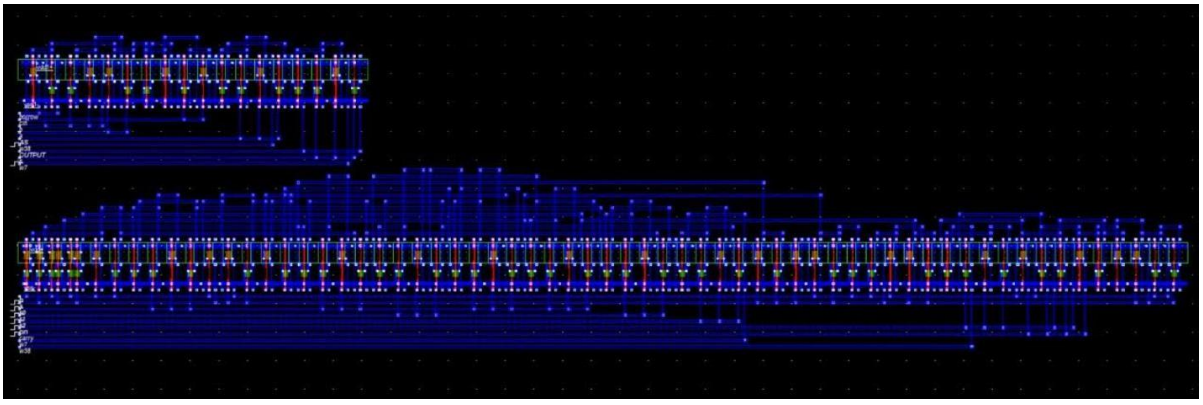

Figure14: Layout of 8bit ALU with proposed 13 T full adder

Conclusion:

A novel internal logic structure has been introduced for the development of full-adder cells.

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The implementation of the new internal logic requires the use of two proposed circuits: XOR and XNOR. The design of the 1-bit full adder incorporates a minimum of 13 transistors, utilizing a combination of pass-transistor and transmission gate logic techniques to demonstrate its benefits. The designs were modeled and evaluated in comparison to other recently reported energy-efficient full adders. They were fabricated using Micro wind 45-nm CMOS technology, operating at supply voltages of 0.8V and 1.2V. The hybrid transistor logic adder demonstrates improved performance regarding average power consumption and power-delay product in comparison to alternative adder architectures. An 8-bit ALU has been developed utilizing the designed adder, showcasing enhancements in power consumption and delay metrics.

The research findings indicate that the proposed adder exhibits a 25% reduction in transistor count compared to CMOS adders. This hybrid transistor logic integrates pass transistor logic with transmission gate logic, achieving a significant overall latency reduction of 30% when compared to earlier systems. The results demonstrate that the proposed adder shows enhanced performance in terms of power consumption and PDP metrics. The designed adder facilitates the creation of an 8-bit ALU, demonstrating improved performance in terms of power consumption and delay.

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